7.1 A 3V 6b Successive-Approximation ADC Using Complementary Organic Thin-Film Transistors on Glass

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Organic thin-film transistors (OTFT) present a new approach to building electronics that can mechanically flex, span large areas, and integrate with polymeric materials. Potential applications include flexible displays, biochemical sensors, and artificial skin. In many applications, OTFTs act as an interface between the physical environment and the digital processors. Yet, a conspicuous absence in the field of organic electronics has been the lack of data converters. Because of the large process variations in OTFT fabrication – often orders of magnitude higher than those in silicon processes [1] – analog OTFT circuits have only been sparsely reported [2-3]. In particular, analog-to-digital converters (ADCs), which rely on component matching for accuracy, have not been demonstrated in an OTFT process thus far. We aim to address such deficiency with the design of this 3V, 6 bit OTFT-based ADC.

Figure 7.1.1 shows a circuit diagram of our ADC. In our organic thin-film process, mismatch distributions showed that capacitors can be made an order of magnitude more precisely than transistors [4]. To leverage this process characteristic, the successive approximation register (SAR) architecture is chosen because its conversion accuracy largely depends on capacitor matching. For a 6 bit conversion, a SAR ADC requires 6 cycles to reach each valid output; however, as most organic sensor applications deal with relatively static signals, speed is not a critical requirement for OTFT data converters. Our ADC contains three main blocks – the digital-to-analog converter (DAC), the comparator, and the digital SAR logic. Because our primary goal is to validate organic analog circuits, the digital SAR logic is implemented in an external field-programmable gate array (FPGA). All interfaces between the FPGA and the ADC are loaded with appropriate capacitances to reflect realistic OTFT conditions.

The DAC utilizes the C-2C structure to reduce the total capacitive load in the circuit. The usual parasitic capacitances that hinder the C-2C structure in silicon CMOS technologies are absent due to the use of glass substrates. Each unit capacitor in the DAC is 280pF, formed by crossing two 200µm wide metal traces, separated by a 6nm-thick dielectric with capacitance C_{ox} = 7fF/µm^2. This unit capacitor size is determined through analyses of capacitor mismatches in [4]. To correct any realistic deviations from the analyses, a two-bit thermometer-coded calibration DAC is included on-chip. The calibration DAC shares the same basic OTFT design as the main DAC, but with 8.75pF unit capacitors. A set of input sampling switches are integrated within the C-2C structure. Because of capacitor leakage, our ADC samples every clock cycle, rather than every six clock cycles as in a typical 6 bit SAR ADC. Although the leakage current density is miniscule [5], the leaked charge can be substantial due to the low operating speed. Re-sampling every clock cycle prevents the leakage errors from accumulating over multiple clock cycles, but results in tracking errors if the rate of change of the input exceeds 1/6 least-significant-bit (LSB) per clock period (530mV/sec at 100Hz clock in our design).

Figure 7.1.2 shows a circuit schematic of the comparator. Several design considerations led to the use of inverter-based gain stages: 1. The comparator must tolerate large device mismatches; 2. The comparator must self-bias to avoid the variability of biasing circuitry; 3. To avoid poor yield, the comparator should be simple. The cascade of inverter-based gain stages satisfies all these conditions. In particular, the inverter is robust against the effects of transistor mismatch because it can automatically self-bias to a high-gain dc operating point. By introducing a two-phase operation, any static offset in the inverter is zeroed as the offset is common to both phases. In the reset phase, the transmission gate shorts the input to the output, establishing the dc operating point, and fixing the bottom plate of C_{S1} to this dc voltage (V_{DC}). Simultaneously, the DAC charges the top plate of C_{S1} to a voltage proportional to the DAC code (V_{DAC}). In the compare phase, the transmission gate shuts off. The DAC then switches to the sampling mode. The voltage on the top plate of C_{S1} is now proportional to the input (V_{IN}); and the voltage on the bottom plate of C_{S1} is now proportional to ($V_{IN} – V_{DAC} + V_{DC}$). The difference ($V_{IN} – V_{DAC}$) is then amplified by the inverter, thus obtaining a comparison between the DAC code and the sampled input.

Analysis shows that the steady-state gain of ac-coupled inverters is simply the ratio of C_S to C_F, where C_S is the input coupling capacitance and C_F is the feedback capacitance between the inverter input and output. In our case, C_F equals the sum of OTFT gate-drain capacitance C_{gd}. To minimize C_F, the n-type OTFT is made to be the same size as the p-type OTFT. This preserves a reasonable steady-state gain despite the typically low n-type mobility in OTFT technology. Although the inverter's steady-state gain is largely independent of the inconsistent OTFT transconductance, it still suffers from variations in C_{gd}. In our thin-film process, soft shadow masks are used to pattern metal contacts on top of the semiconductors. The softness prevents damage to the semiconductor, but is prone to misalignment. To tolerate alignment errors, large overlaps exist between the gate metal and the source-drain metals, leading to large C_{gd} – nominally 70pF for a 500µm wide OTFT. Depending on the amount of misalignment, C_{gd} can vary from 0pF to 140pF over process. To minimize gain variations caused by this fluctuation in C_{gd}, the p-type OTFT is placed anti-symmetrical to the n-type OTFT. Any increase in C_{gd} of one OTFT is compensated by an equal decrease in C_{gd} of the opposing OTFT, resulting in a constant total C_{gd} and a constant gain. (Because C_S is fabricated from intersecting metal traces, it is immune to x-y mask misalignment.) Figure 7.1.3 shows a cross-sectional view of the OTFT and the anti-symmetrical inverter layout.

For a 2V full-scale range (FSR) and 0.5 LSB precision, the total comparator gain needs to be greater than 96. From a detailed circuit analysis, it follows that 3 gain stages are required. A 4th stage is added to shift the output dc voltage closer to $V_{DD}/2$ = 1.5V. Figure 7.1.4 shows the measured comparator output as the DAC increments from code 17 to 21 while sampling V_{in} = 1.55V at 100Hz. A clear low-to-high transition occurs between code 18 and 19, indicating that the 1.55V input is converted to code 19.

Figure 7.1.5 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC at the sampling frequency f_s = 10Hz, with the maximum DNL = -0.6 LSB, and the maximum INL = 0.6 LSB. As f_s increases to 100Hz, the maximum DNL worsens to 1.5 LSB, while the maximum INL worsens to -3 LSB. At f_s = 100Hz, the power consumption of the ADC (excluding FPGA) is 3.6µW, of which the comparator consumes 2.9µW.

Figure 7.1.6 shows a photograph of the ADC on a glass substrate. (The substrate sits on a black background to enhance visibility.) The ADC includes 27 p-type OTFTs, 26 n-type OTFTs, and 19 capacitors. Total area measures 28mm x 22mm. The fabrication process is based on that reported in [4]. The measured p-type and n-type mobilities are 0.5cm^{2}V^{-1}s^{-1} and 0.02cm^{2}V^{-1}s^{-1}, respectively. The ADC is tested in ambient air.

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[5] H. Klauk et al., "Ultralow-power organic complementary circuits," *Nature*, vol. 445, pp. 745-748, Feb. 2007.

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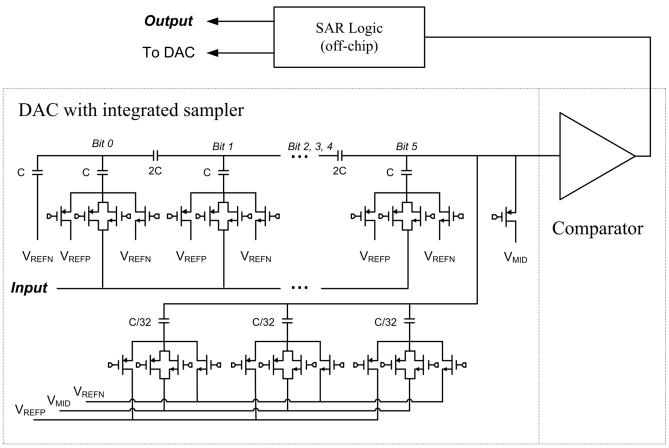

Figure 7.1.1: ADC block diagram with detailed DAC circuit.

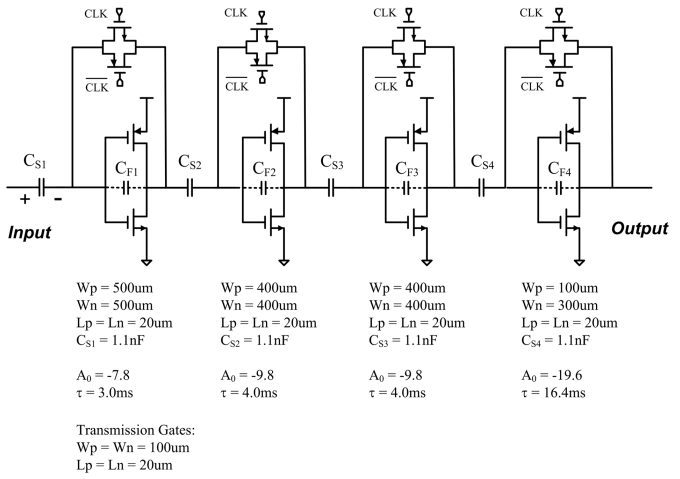

Figure 7.1.2: Comparator circuit and device parameters.

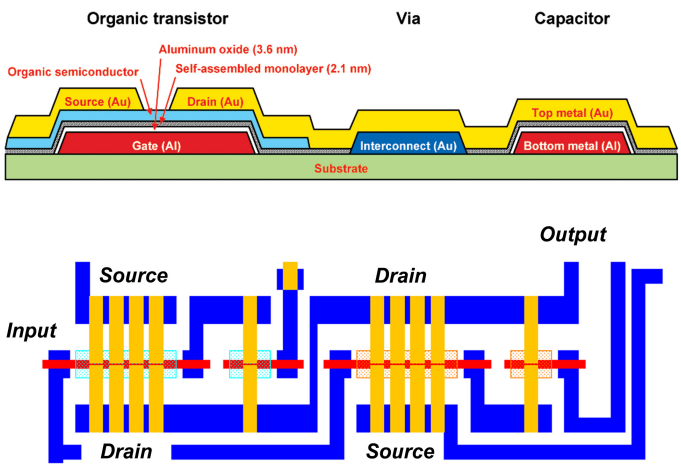

Figure 7.1.3: Device cross-sections and anti-symmetric inverter layout.

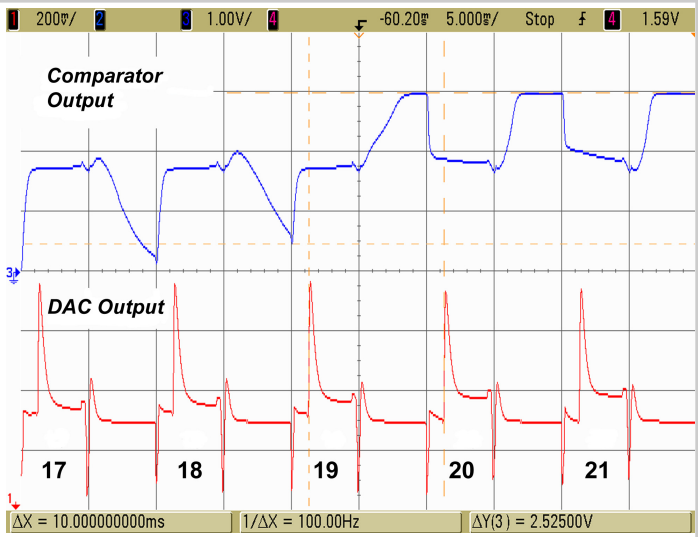

Figure 7.1.4: Measured comparator output and DAC output.

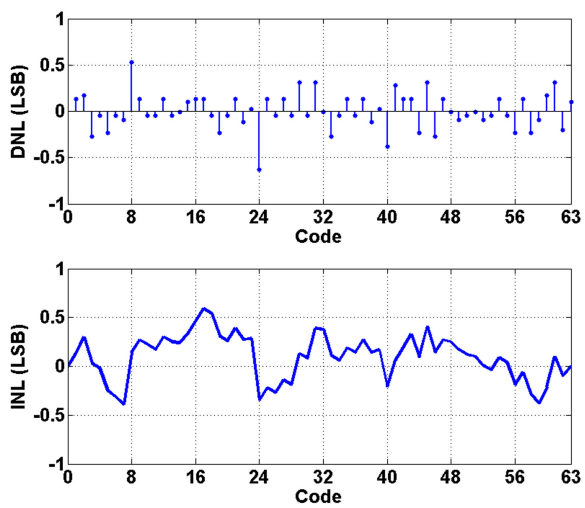

Figure 7.1.5: Measured DNL and INL.

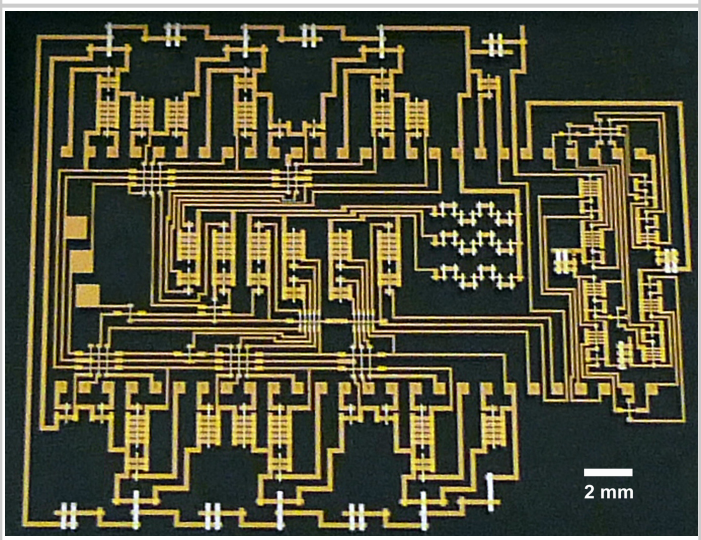

Figure 7.1.6: Photograph of ADC on glass substrate.