Low-Power Organic Light Sensor Array Based on Active-Matrix Common-Gate Transimpedance Amplifier on Foil for Imaging Applications

Samar Elsaegh, Clemens Veit, Ute Zschieschang, Mohammad Amayreh, Florian Letzkus, Holger Sailer, Michael Jurisch, Joachim N. Burghartz, Uli Würfel, Hagen Klauk, Hans Zappe, and Yiannos Manoli, *Life Fellow, IEEE*

***Abstract*— This article presents a 57.6-μW mechanically flexible active-matrix imaging system based on a 4 × 5 array of light sensors, each composed of a photodetector (PD) using a light-sensitive organic polymer and a transimpedance amplifier (TIA) based on organic thin-film transistors and integrated thin-film carbon resistors. The PDs and the electronics are fabricated on separate plastic films and integrated into a system. Two different topologies for the TIA are designed, implemented, and characterized. The first topology is a self-biased TIA based on a gain-boosted operational amplifier (op-amp), providing an open-loop dc gain of 41.3 dB. This op-amp-based TIA, with a feedback resistor, provides stable current-to-voltage conversion (0–100 μA and 2.0–3.7 V) at frequencies up to 300 Hz. The second topology is a low-power gain-boosted common-gate (GB CG) TIA that performs current-to-voltage conversion with a nonlinearity as small as ±0.3% within a bandwidth of 1 kHz. The output voltages of the light sensors are read and converted into a 4 × 5 pixel gray-scale image displayed on a computer monitor to visualize the functionality of the system.**

***Index Terms*— Gain-boosted common-gate transimpedance amplifier (GB CG TIA), operational amplifier (op-amp), organic imaging, organic light sensor, organic photodetector (OPD), organic thin-film transistors (TFTs), transimpedance amplifier (TIA).**

I. Introduction

THERE is a great scientific and commercial interest in large-area, mechanically flexible, and possibly disposable electronic systems, such as displays and sensors, for medical, security, and consumer applications. Using complementary metal–oxide–semiconductor field-effect transistor (CMOS-FET) technologies for the development of such large-area sensor systems, including their readout backplanes, requires high costs and poses additional challenges for integration. Therefore, other options, such as organic thin-film transistor (TFT) technologies, have lately attracted significant research interest for the fabrication of large-area sensor arrays. This is due to their simple and, hence, low-cost manufacturing at moderate temperatures (usually around or below 100 °C) on large-area flexible substrates, such as plastics and paper [1]. TFT-based sensors have been reported for detecting mechanical strain [2], [3], spatial distribution of pressure [4], biological electrical activity [5], biological compounds [6], [7], and photo intensity [8]–[12].

Large-area photodetector (PD) systems are essential for many industrial applications, such as emotional lighting applications [9], optical/touch sensors [13], and imaging applications [10], [14]–[16]. The simplest implementation is an array of passive pixels in which a single-access TFT is integrated into each pixel [14]–[16]. For systems more demanding in terms of detectivity or image quality, an active-pixel design is desirable where a specifically designed signal-conditioning circuit is integrated into each pixel. For example, systems for low-light-intensity applications benefit greatly from a charge-amplification circuit integrated into each pixel [11], [12], since the minimum detectable signal is limited by the array's dataline-capacitance noise.

Regardless of the pixel design, PD systems also require readout circuits to perform charge-to-voltage conversion in order to facilitate further signal processing. One possibility is the charge-integration readout circuits that have shown excellent performance in a variety of applications [11], [12], [17]. However, these circuits are difficult to optimize for systems in which the PDs generate large output currents. For example, in [10], an integrating capacitor with a capacitance of up to 4.7 nF was required in order to limit the output-voltage swing to 1.8 V. In addition, the design of a charge-integration readout circuit meets some challenges, such as switching and timing requirements. As an alternative to charge-integration readout circuits for large-area PDs, transimpedance amplifiers (TIAs) have been suggested. TIAs are able to perform current-to-voltage conversion with excellent linearity and can be more

Manuscript received December 11, 2019; revised March 20, 2020; accepted April 27, 2020. Date of publication May 21, 2020; date of current version August 26, 2020. This article was approved by Associate Editor Pui-In Mak. This work was supported in part by the Gisela and Erwin Sick scholarship and in part by the German Research Foundation (DFG) under Grant KL 2223/6-1, Grant KL 2223/6-2 (SPP FFlexCom), and Grant KL 2223/7-1. *(Corresponding author: Samar Elsaegh.)*

Samar Elsaegh, Mohammad Amayreh, and Hans Zappe are with IMTEK, University of Freiburg, 79110 Freiburg, Germany (e-mail: samar.elsaegh@imtek.uni-freiburg.de).

Clemens Veit and Uli Würfel are with the Fraunhofer Institute for Solar Energy Systems (ISE), 79110 Freiburg, Germany.

Ute Zschieschang and Hagen Klauk are with the Max Planck Institute for Solid State Research, 70569 Stuttgart, Germany.

Florian Letzkus, Holger Sailer, Michael Jurisch, and Joachim N. Burghartz are with the Institut für Mikroelektronik (IMS CHIPS), 70569 Stuttgart, Germany.

Yiannos Manoli is with IMTEK, University of Freiburg, 79110 Freiburg, Germany, and also with Hahn-Schickard, 78052 Villingen-Schwenningen, Germany.

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2020.2993732

TABLE I

FEW IMPORTANT PROPERTIES OF TFTS BASED ON ORGANIC AND INORGANIC SEMICONDUCTORS AND OF SINGLE-CRYSTALLINE SILICON MOS-FETS

	Silicon MOS-FETs	Hydrogenated amorphous silicon (a-Si:H) TFTs	Low-Temperature polycrystalline silicon (LTPS) TFTs	Indium-gallium-zinc-oxide (IGZO) TFTs	Organic TFTs
Process temperature [°C]	> 800	200 to 300	450 to 550	20 to 200	20 to 200
Substrate	silicon	glass	glass, polyimide	glass, plastics	glass, plastics, paper
Electron mobility in n-channel transistors [cm^2/Vs]	400 to 800	~1	100 to 200	10 to 50	0.1 to 1
Hole mobility in p-channel transistors [cm^2/Vs]	100 to 200	<0.1	50 to 100	n/a	1 to 10
Typical channel length [µm]	~0.01	~1	~1	~1	~1
Transit frequency [Hz]	$>10^{11}$	$>10^{6}$	$>10^{8}$	$>10^{8}$	$>10^{7}$
Parameter uniformity	excellent	excellent	good	excellent	poor
Off-state leakage [A/µm]	10^{-10}	10^{-15}	10^{-14}	10^{-15}	10^{-15}
Bias-stress stability	excellent	good	excellent	very good	poor
References	[18–20]	[21, 22]	[23–25]	[26, 27]	[28–30]

easily designed to handle high input currents. TIAs based on a high-gain operational amplifier (op-amp) in a resistor-feedback configuration have been fabricated using organic or inorganic TFTs [8], [10]. In contrast to charge-integration readout circuits, the input-referred noise of a TIA is not amplified toward the output, and the linearity of well-designed TIAs can be better than that of state-of-the-art charge-integration circuits by at least a factor of three [10].

However, both the performance (gain, bandwidth, and power consumption) and the reproducibility of organic-TFT-based op-amps tend to be quite poor due to the small charge-carrier mobility of organic TFTs, the inherent device-to-device variations, as well as the lack of *n*-channel organic TFTs with sufficient performance and stability. Table I provides a summary of a few important properties of TFTs based on organic and inorganic semiconductors and of single-crystalline silicon MOS-FETs. The comparison illustrates the challenges associated with the design of high-performance analog circuits based on TFTs, rather than silicon MOS-FETs.

Here, we present PD readout circuits designed specifically for the detection of ambient light, the illuminance of which varies over three orders of magnitude, from about 10 lx at twilight to about 10 klx at full daylight. This wide illuminance range presents a significant challenge for the design of ambient-light detectors with usefully large resolution. The TIA circuits proposed here address this challenge with their ability to operate over a wide range of input currents (0–100 μA) with excellent linearity and a resolution of 9.8 bits, which corresponds to a minimum resolved illumination as low as 12 lx. To be able to provide a system demonstration of this capability, a 4×5 array of very-large-area PDs (9 mm^2) was designed to deliver a current of 100 μA at an illuminance of 10 klx despite their low responsivity. The optimum size of the PDs will obviously depend on the specifications of the PDs and the system. The PD array and the TIA array were fabricated on two separate sheets of flexible plastic films. The output signals of the 20 sensors are read and interpreted into a 4×5 gray-scale-pixel screen using masks with various structures.

This article is organized as follows: Section II presents the design, fabrication, and characterization of the organic PDs.

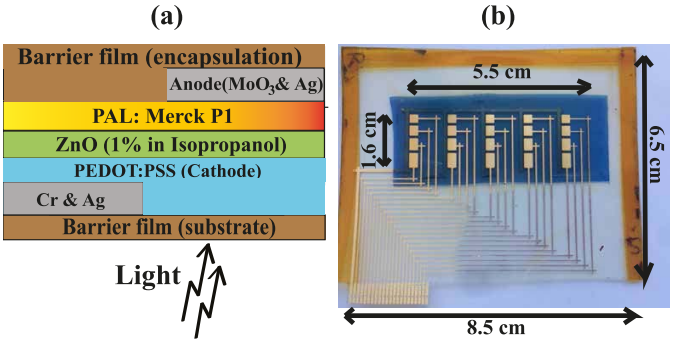


Fig. 1. (a) Schematic cross section of the OPDs. (b) Photograph of a completed PD array.

The implementation and analysis of the two proposed TIA topologies are discussed in Section III, highlighting the advantages and disadvantages of each. Section IV summarizes the overall system assembly and the measurements, and Section V provides a conclusion.

II. ORGANIC PHOTODETECTORS (OPDS)

The OPD array was developed at the Fraunhofer Institute for Solar Energy Systems (ISE), Freiburg, Germany. A schematic cross section of the organic PDs is shown in Fig. 1(a). A 3M ultra-barrier film is used as the flexible transparent substrate. The cathode is a layer of poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS; Clevios FHC Solar) deposited by spin-coating and annealed at a temperature of 100 °C for 10 min in ambient air. As an electron-selective charge-extraction layer, zinc oxide (ZnO) is deposited from a nanoparticle suspension (Avantama N11; 1 % in 2-propanol) by spin-coating, followed by annealing at a temperature of 120 °C for 10 min. This is followed by the photoactive layer comprising the photosensitive polymer Merck P1 blended with a fullerene derivative. This layer was also deposited by spin-coating and annealed at a temperature of 110°C for 10 min under N_2. It forms an interpenetrating network of the polymer P1 as the donor and the fullerene derivative as the acceptor usually referred to as bulk heterojunction [31]–[33]. This intimate mixture of both components

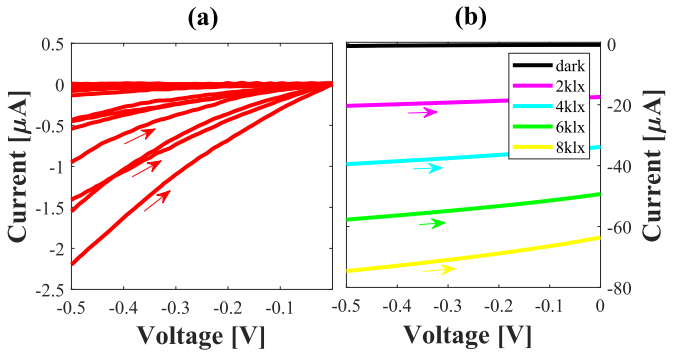


Fig. 2. (a) Current–voltage characteristics under dark condition of 15 OPDs, measured in ambient air, in the voltage range of interest. (b) Current–voltage characteristics of a PD cell under illumination with illuminance ranging from 0 to 8 klx in steps of 2 klx.

in the photoactive layer enables sufficient light absorption by simultaneously ensuring a high rate of exciton dissociation and, thus, generation of free charge carriers (electrons in the acceptor and holes in the donor) at the donor/acceptor interfaces. This bulk-heterojunction device structure results in a responsivity of 1 μA/klx·mm^2 ($\sim$128 mA/W). Finally, 10-nm-thick molybdenum(VI) oxide (MoO_3) and 100-nm-thick silver (Ag) were deposited by thermal evaporation in a vacuum as a hole-selective charge-extraction layer and anode, respectively. This top electrode was patterned using a shadow mask.

Encapsulation of the PD array was accomplished by bonding a 3M ultra-barrier-film using Delo Katiobond LP655. All fabrication steps were performed in a nitrogen-filled glove box in order to prevent water and oxygen from degrading the photoactive layer. This device structure was chosen for its ease of the process and because it eliminates the requirement for the deposition and patterning of indium tin oxide (ITO). In addition to the described materials, Fig. 1(a) shows a support structure which consists of a stack of 5-nm-thick chromium (Cr) and 100-nm-thick Ag deposited by thermal evaporation under high vacuum. This support structure is required due to the limited conductivity of the organic cathode (PEDOT:PSS) and has, however, no other function. A photograph of a completed PD array is shown in Fig. 1(b).

Each PD cell occupies an area of 0.1 cm^2, which results in an output current of 100 μA when illuminated with an illuminance of 10 klx, corresponding to an illuminance-to-current conversion ratio of 10 μA/klx. The output capacitance of the PD cells measured at a dc bias of zero and with a frequency of 100 Hz under illumination is between 0.7 and 2.2 nF. This output capacitance affects the stability of the readout TIA and must, therefore, be considered in the circuit design, as will be discussed in Section III. The current–voltage characteristics of 15 PD cells within the 4×5 array measured in the dark are shown in Fig. 2(a). The measured illumination response of a PD cell is shown in Fig. 2(b).

The dark current density, calculated from Fig. 2(a), ranges from 1 to 4 nA/mm^2 at a reverse bias of 0.01 V and from 4 to 210 nA/mm^2 at a reverse bias of 0.5 V. In Fig. 2(b), the measured PD shows a maximum responsivity nonlinearity of 12% of its average value at a reverse bias of 0.5 V.

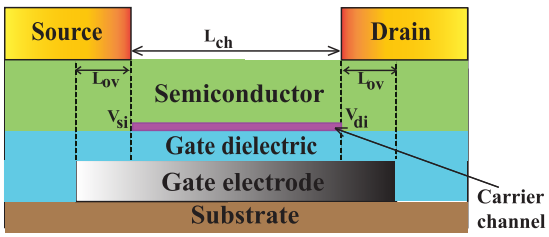


Fig. 3. Schematic cross section of the organic TFTs.

Furthermore, it can be seen from the figure that the output resistance (apparent shunt resistance) decreases with increasing illuminance, from 360 kΩ in the dark to 180 kΩ at a low illuminance of 2 klx and 50 kΩ at an illuminance of 8 klx. This effect can be ascribed to the rather low charge-carrier mobility of the photoactive layer, which has been investigated thoroughly in previous work [34]. This relatively small output resistance results in a mismatch error of $\pm$7.7% of the output voltage produced by the TIA among the 20 sensor cells due to the fact that the input voltage of the circuits can vary by 0.5 V, as shown in Section III. This output-voltage error is accounted for by multiplying by a calibration matrix (CM) during the reading of the output voltages into the screen pixels, as will be discussed in Section IV.

III. Transimpedance Amplifiers (TIAs)

The TIA circuits proposed in this article were implemented using organic p-channel TFTs fabricated in the inverted staggered architecture using the commercially available air-stable small-molecule semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) or its derivative DPh-DNTT [36]. Monolithically integrated thin-film resistors were implemented using vacuum-deposited carbon with a thickness of 20 nm [37]. The circuits were fabricated on flexible polyethylene naphthalate (PEN) substrates. Gold (Au) interconnects, aluminum (Al) gate electrodes, the organic semiconductor, and the Au source/drain contacts were deposited by thermal evaporation or sublimation in vacuum, with a thicknesses of 20–30 nm each. The gate dielectric is a combination of 3.6-nm-thick oxygen-plasma-grown aluminum oxide (AlO_x) and a 1.7-nm-thick tetradecylphosphonic-acid self-assembled monolayer (SAM) and has a unit-area capacitance of 0.7 μF/cm^2. Aluminum oxide with a thickness of 100 nm deposited by electron-beam evaporation was used as an interlayer dielectric. All layers were patterned using silicon stencil masks [38], except for the AlO_x/SAM gate dielectric that grows selectively on the Al gate electrodes. A schematic cross section of the organic TFTs is shown in Fig. 3.

The TFTs have a channel length (L_{ch}) of 4 or 20 μm, gate-to-source and gate-to-drain overlaps (L_{ov}) of 20 μm, and effective charge-carrier mobilities between 1 and 3 cm^2/Vs depending on the semiconductor and the channel length. The subthreshold swings and ON/OFF current ratios are 90 mV/decade and 10^8, respectively. The thin-film resistors have a length of 240–520 μm, a width of 40 μm, and a sheet resistance of 1 MΩ/sq.

TABLE II
ORGANIC-TFT PARAMETERS EMPLOYED IN THE CIRCUIT SIMULATIONS USING THE COMPACT MODEL PROPOSED IN [35]

Parameter	Definition	Value	Units
μ_o	Intrinsic charge-carrier mobility	3 to 3.3	[cm^2/Vs]
V_{th}	Threshold voltage	-1 to -1.5	[V]
C_{diel}	Gate-dielectric capacitance per unit area	0.7	[μF/cm^2]
W_{fringe}	Extension width added to the channel width to account for the fringe current	10	[μm]
V_T	Thermal voltage	25.9	[mV]
J_{os}	Current density underneath the gate-to-source overlap	1800	[A/m^2]
η_s	Non-ideality factor at the source contact	21.45	-
P_{snorm}	Charge-normalization power factor at the source contact	0.8	-
J_{od}	Current density underneath the gate-to-drain overlap	27250	[A/m^2]
η_d	Non-ideality factor at the drain contact	4	-
P_{dnorm}	Charge-normalization power factor at the drain contact	0.8	-

The circuits were designed and simulated with the help of the organic-TFT compact model proposed in [35] using (1)–(3) that describe the current–voltage characteristics of the channel, the source contact, and the drain contact, respectively

$$I_{sd} = \frac{1}{2}\frac{W_{ch}+W_{fringe}}{L_{ch}}\mu_0 C_{diel}(1+\lambda(V_{si}-V_{di})) \\ [(V_{si}-V_g+V_{th})^2-(V_{di}-V_g+V_{th})^2] \quad (1)$$

$$I_{sd} = L_{ov}J_{os}(W_{ch}+W_{fringe})\left(e^{\frac{V_s-V_{si}}{\eta_s V_T}}-1\right)(V_{si}-V_g+V_{th})^{P_{snorm}} \quad (2)$$

$$I_{sd} = L_{ov}J_{od}(W_{ch}+W_{fringe})\left(e^{\frac{V_{di}-V_d}{\eta_d V_T}}-1\right)(V_{di}-V_g+V_{th})^{P_{dnorm}} \quad (3)$$

where I_{sd} is the current flowing through the source and the drain terminals of the TFT. V_s, V_d, and V_g are the potentials applied at the source, the drain, and the gate nodes, respectively. V_{si} and V_{di} are the voltages of the gate-field-induced carrier channel at the location closest to the source contact and the drain contact, respectively. L_{ch} and W_{ch} are the channel length and width. The definitions of the model parameters and their corresponding values are summarized in Table II.

Fig. 4 shows the measured and simulated output and transfer characteristics of TFTs with L_{ch} of 100 and 4 μm and W_{ch} of 200 μm, confirming the good agreement between measurement and simulation results.

The design of the TIA has to meet a number of requirements. The circuit should have low power consumption, yet be able to pass large currents in order to cover a wide range of illuminance required for ambient light detection (up to 10 klx) with high resolution. In addition, the circuit must have a low input impedance to ensure that the input current (I_{in}) depends only on the illuminance and not on the input voltage applied to the PD (V_{in}). This is particularly problematic since OPDs often have a relatively small output impedance, e.g., 71 kΩ in [39]. For the PDs used here, with an output impedance of 90 kΩ at an illuminance of 4 klx, the input impedance of the TIA must, therefore, be smaller than 2.5 kΩ in order to keep the light-to-current linearity error below ±2.5%. The second reason for designing the TIA with a low input impedance is to avoid loading the PD output capacitance with the TIA input resistance, which would negatively affect the response time of the PD. In this section, we discuss the design and fabrication of the conventional op-amp TIA topology and compare it to the gain-boosted common-gate TIA (GB CG TIA) topology proposed in [40].

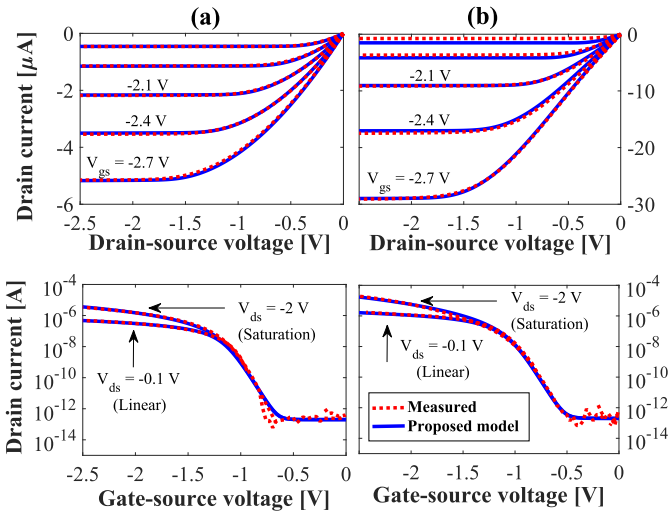


Fig. 4. Measured and simulated output (top row) and transfer (bottom row) characteristics of a TFT with (a) L_{ch} = 100 μm and W_{ch} = 200 μm and (b) L_{ch} = 4 μm and W_{ch} = 200 μm.

A. Op-Amp-Based TIAs

Fig. 5 shows the circuit schematic of the op-amp-based TIA implemented using p-channel organic TFTs and thin-film carbon resistors. The TIA is composed of an op-amp with the resistor R_{FB} in a feedback configuration. The op-amp consists of a self-biased differential stage with a resistive load. To meet the requirements for low power consumption and high gain, the self-biased differential stage is designed to operate with

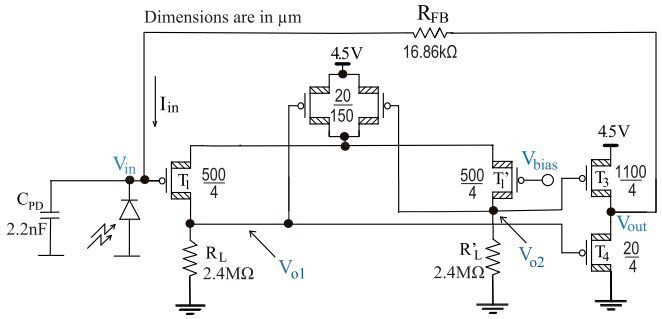


Fig. 5. Circuit schematic of an op-amp-based TIA without gain-boosting.

a total current of 1.5 μA. By designing an output stage with zero power consumption in the dark, a single-ended op-amp is realized, which is capable of handling currents up to 100 μA from the PD through the large-channel-width transistor T_3.

The closed-loop transfer function (TF) of the op-amp feedback configuration can be written as

$$\mathrm{TF} = \frac{R_{\mathrm{FB}}}{1 + 1/A_{\text{op-amp}}} \tag{4}$$

where $A_{\text{op-amp}}$ is the open-loop op-amp gain. Sufficiently large op-amp gain guarantees that the TF is determined mainly by the resistance of the feedback resistor R_{FB}. In addition, a larger $A_{\text{op-amp}}$ implies that the TF is less sensitive to variations of the value of $A_{\text{op-amp}}$ and the parameters affecting it according to the following equation:

$$\frac{\partial \mathrm{TF}}{\partial A_{\text{op-amp}}} = \frac{R_{\mathrm{FB}}}{1 + A^2_{\text{op-amp}}}. \tag{5}$$

Thus, a large op-amp gain is important for providing sufficient linearity of the TIA. However, due to the small carrier mobility of organic TFTs, op-amps based on organic TFTs often suffer from small dc gain at low power consumption. To boost the dc gain while maintaining a low power consumption, a positive feedback is added to the differential stage. This concept is illustrated in Fig. 6(a). As the output voltage (V_{out}) increases in response to an increase in the input current (I_{in}), the input voltage (V_{in}) decreases due to the finite dc gain of the op-amp. This undesirable reduction in V_{in} is counteracted by the positive feedback circuit, which increases the equivalent bias voltage and, thereby, stabilizes V_{in}, resulting in higher overall dc gain.

The positive feedback circuit is implemented by adding the cross-coupled transistors T_5 and T_5' to the differential stage, as shown in Fig. 6(b). Since the output resistances of T_1 and T_1' (in the range of 125 MΩ) are much larger than the load resistance ($R_L = 2.4$ MΩ), the working principle of the gain-boosted op-amp-based TIA can be explained through the simplified small-signal block diagram shown in Fig. 7.

From Fig. 7, the overall small-signal gain of the gain-boosted op-amp-based TIA can be estimated as follows:

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{-2gm_1 R_L}{1 - gm_5 R_L}. \tag{6}$$

To ensure stability, the gain of the positive feedback network ($gm_5 \cdot R_L$) must be smaller than unity according to the unity-gain criterion. This can be guaranteed by choosing the

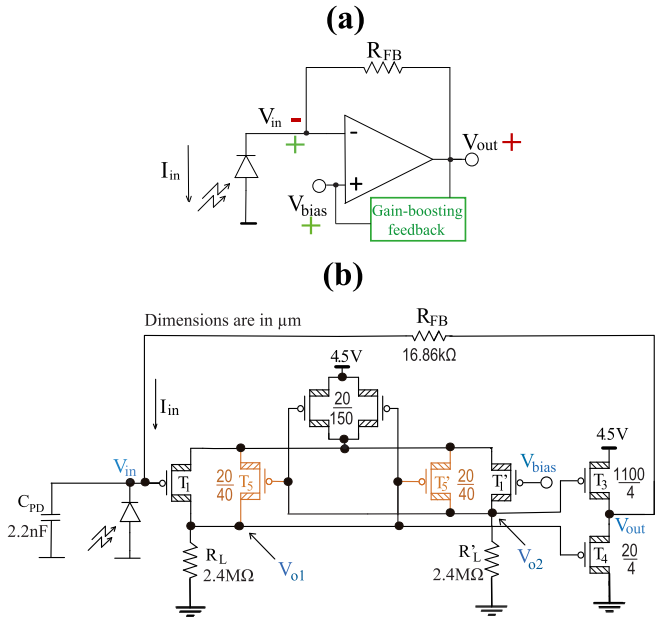


Fig. 6. Gain-boosted op-amp-based TIA. (a) Concept. (b) Circuit schematic.

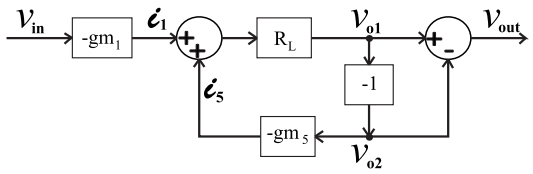


Fig. 7. Block diagram to describe the simplified small-signal model of the gain-boosted op-amp-based TIA.

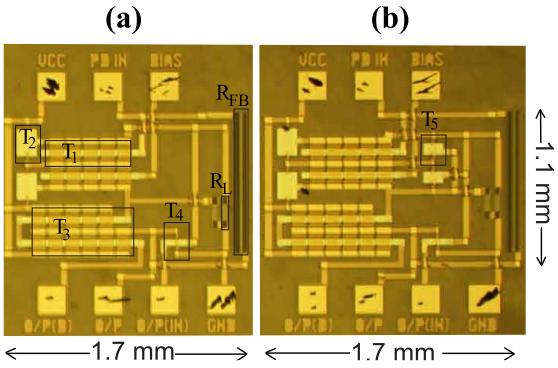


Fig. 8. Photographs of the op-amp-based TIAs. (a) Without gain-boosting and (b) with gain-boosting, fabricated on a flexible plastic substrate using organic TFTs and thin-film carbon resistors.

aspect ratio of T_5 (W_5/L_5) to be smaller than 1. To account for the non-linear parasitic contact resistances, fringe currents, and process variations, the aspect ratio of T_5 was set to 0.5 ($W_5/L_5 = 20$ μm/40 μm).

Fig. 8 shows the photographs of the op-amp-based TIA implemented using p-channel organic TFTs and thin-film carbon resistors.

Fig. 9 shows the measured and simulated dc voltages present at the circuit nodes V_{in}, V_{out}, V_{o1}, and V_{o2} of the op-amp-based TIAs without gain-boosting (see Fig. 5) and

TABLE III

COMPARISON OF THE OP-AMP-BASED TIA WITH AND WITHOUT GAIN-BOOSTING, ACROSS THE RANGE OF INPUT CURRENTS FROM 25 TO 100 μA

Design base	Op-amp dc gain [dB]	Transimpedance nominal value [kΩ]	$(R_{FB}-R_{nomianl})/R_{FB}$ [%]	Transimpedance nonlinearity [%]	Circuit active area [mm^2]	Power consumption [μW]
Op-amp TIA	31.66	16.255	3.6	±1.2 %	1.75	6.75
GB op-amp TIA	41.3	16.785	0.445	±0.45 %	1.87	7.2

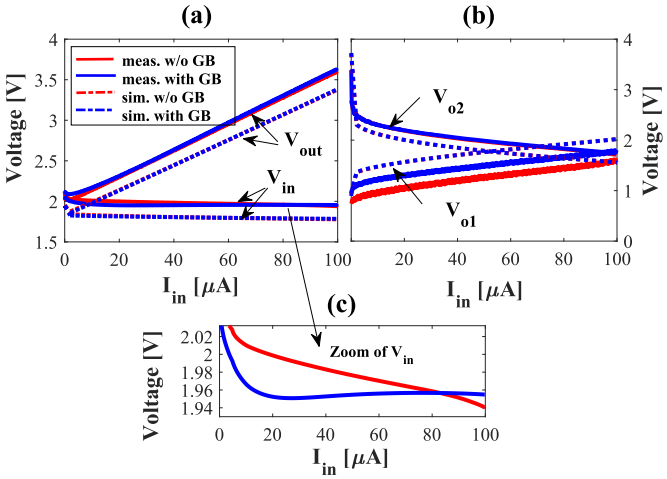


Fig. 9. Measured (continuous lines) and simulated (dotted lines) voltages of the op-amp-based TIA without gain-boosting from Fig. 5 (red) and the gain-boosted op-amp-based TIA from Fig. 6 (blue) that are present at the following circuit nodes: (a) V_{in} and V_{out}, (b) V_{o1} and V_{o2}, and (c) V_{in}. The benefit of the gain-boosting concept in stabilizing the input voltage is clearly seen.

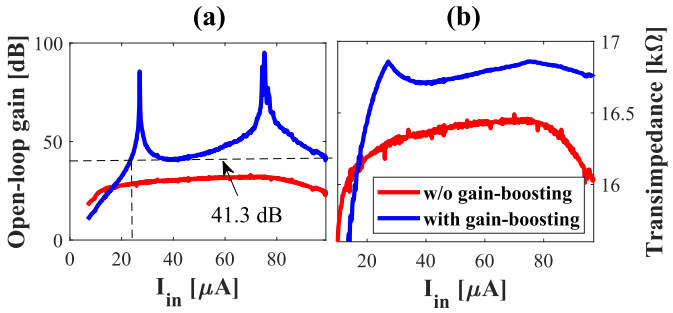


Fig. 10. (a) Open-loop dc gain and (b) transimpedance (closed-loop TF) of the op-amp-based TIA without gain-boosting (red) and the gain-boosted op-amp-based TIA (blue) as a function of the input current, calculated from the measurement data in Fig. 9(a).

with gain-boosting (see Fig. 6). The voltages are plotted for a sweep of the input current from 0 to 100 μA. Fig. 9(c) clearly shows the efficiency of the positive-feedback configuration in suppressing the variations of V_{in}. The unavoidable device-to-device variations lead to an input-offset voltage of 0.15 V.

From the measurement data in Fig. 9(a), we have calculated the dc open-loop gain (v_{out}/v_{in}) and the closed-loop transimpedance (v_{out}/i_{in}) and plotted them as a function of the input current in Fig. 10(a) and (b). As can be seen, the conventional op-amp-based TIA has a maximum open-loop dc gain of 31.66 dB, which is too small to provide adequate linearity of the transimpedance system. Our gain-boosting technique enhances the open-loop dc gain by at least 10 dB so that a

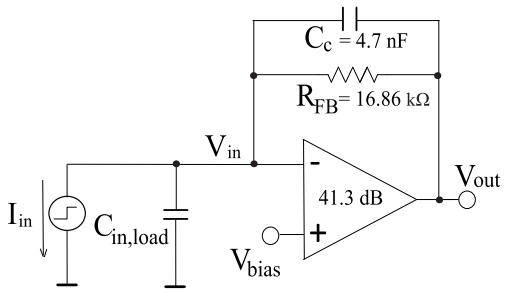


Fig. 11. Schematic of the setup for investigating the stability of the gain-boosted op-amp-based TIA with respect to a sudden increase in the input current by 100 μA.

minimum open-loop gain of 41.3 dB is maintained for input currents from 25 to 100 μA (and a minimum open-loop gain of 50 dB for input currents from 65 to 88 μA). Due to the higher open-loop dc gain produced by the gain-boosting configuration, the transimpedance nonlinearity is improved by about ±0.75% around its nominal value, which is only marginally smaller than R_{FB}, with a 6.7% increase in power consumption. Table III summarizes the performance of the two op-amp-based TIA architectures with respect to their linearity error, occupied active area and power consumption.

The device-to-device variations on the same substrate are approximately as follows: ±5% for the effective carrier mobility of the TFTs, ±1.2% for the threshold voltage of the TFTs, ±8.75% for the transconductance of the TFTs (see [38]), and ±10% for the value of the resistors (see [37]). These variations lead, in the worst case, to a decrease of the op-amp gain by around 4 dB. The dependence of this gain reduction on the parameter variations can be evaluated using the following equation:

$$\Delta A_{\text{op-amp}} = 2gm_1\Delta R_L + 2R_L\Delta gm_1. \tag{7}$$

This gain reduction results in a variation of the transimpedance value (TF) by around ±11.7% according to the following equation:

$$\frac{\Delta \text{TF}}{\text{TF}} = \frac{\Delta R_{\text{FB}}}{R_{\text{FB}}} + \frac{1}{gm_1 R_L}\left[\frac{\Delta R_L}{R_L} + \frac{\Delta gm_1}{gm_1}\right]. \tag{8}$$

To verify the stability of the gain-boosted op-amp-based TIA, we have measured the response of the input node (V_{in}) and the output node (V_{out}) to a sudden increase in the input current by 100 μA. The setup for this measurement is schematically shown in Fig. 11. A capacitor $C_{in,load}$ with a capacitance equivalent to the capacitance provided by the organic PD is connected at the input node. This capacitance is in the range from 0.7 to 2.2 nF, as discussed in Section II. The current-step response of the gain-boosted op-amp-based

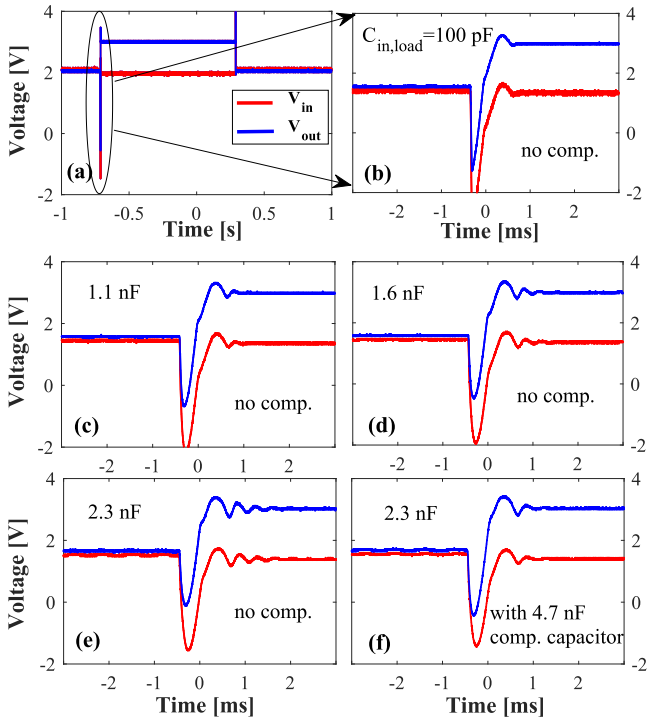


Fig. 12. Measured response of the input and the output nodes of the gain-boosted op-amp-based TIA in a closed-loop configuration to a sudden increase in the input current by 100 μA for different values of the capacitance $C_{\text{in,load}}$ connected at the input of the amplifier. (a) and (b) $C_{\text{in,load}}$ = 100 pF, which corresponds to the capacitance of the test setup (probe and oscilloscope). (c) $C_{\text{in,load}}$ = 1.1 nF. (d) $C_{\text{in,load}}$ = 1.6 nF. (e) $C_{\text{in,load}}$ = 2.3 nF. (f) $C_{\text{in,load}}$ = 2.3 nF with an additional compensation capacitor of 4.7 nF connected between the input and the output nodes of the op-amp to ensure a phase margin of at least 30°.

TIA for different values of $C_{\text{in,load}}$ is summarized in Fig. 12. Initially, a value of $C_{\text{in,load}}$ = 100 pF is used, which is the capacitance associated with the test setup (probe and oscilloscope). The large undershoot observed in Fig. 12(a) and (b) is due to the extremely short rise time of the applied current step, which discharges the capacitance available at the input node (C_{in}) before the op-amp is able to respond. Such a sudden increase in current is, however, not expected in the imaging system discussed in the following, so the undershoot observed here will not be a problem. From the slope of the undershoot, the input capacitance of the op-amp is estimated to be 0.8 nF, according to the following equation:

$$I_{\text{in}} = C_{\text{in}} \frac{\partial V_{\text{in}}}{\partial t}. \tag{9}$$

Fig. 12(b)–(e) shows that the gain-boosted op-amp-based TIA is stable over a range of $C_{\text{in,load}}$ from 0 to 2.3 nF even without an additional compensation capacitor (C_c) and that it settles within less than 1 ms, even in the worst case scenario ($C_{\text{in,load}}$ = 2.3 nF). The results also show that the stability of the TIA degrades with increasing $C_{\text{in,load}}$, as indicated by the increased ringing of the response with increasing $C_{\text{in,load}}$. This is due to the additional pole created by the series connection of the feedback resistor R_{FB} and the input capacitance $C_{\text{in,load}}$. For a large $C_{\text{in,load}}$, this pole moves closer to the dominant pole of the op-amp, which leads to a reduction in the phase margin. A compensation capacitor (C_c) with a capacitance of 4.7 nF is

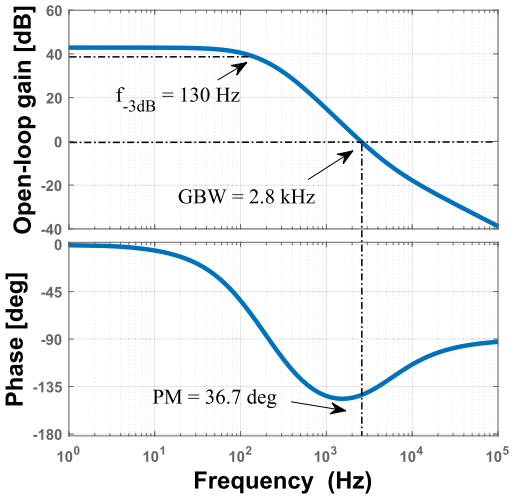


Fig. 13. Open-loop Bode plot of the gain-boosted op-amp-based TIA loaded with the feedback circuit and the compensation capacitor C_c, deduced from the measured step response shown in Fig. 12(f). (a) Open-loop gain as a function of frequency. (b) Phase as a function of frequency.

externally connected between the input and the output nodes in order to compensate for this additional pole and to ensure a phase margin (PM) of at least 30° for the entire range of expected PD capacitances (0.7 to 2.2 nF). As can be seen in Fig. 12(f), the additional capacitance C_c = 4.7 nF indeed decreases the ringing.

According to [41], the phase margin of an underdamped second-order system can be estimated from the number of oscillations in the closed-loop step response. Using the software program MATLAB, we have, thus, generated an underdamped second-order system whose step response matches the measured step response shown in Fig. 12(f). From the results of this analysis, the open-loop Bode plot of the gain-boosted op-amp-based TIA loaded with the equivalent feedback circuit, including $C_{\text{in,load}}$ = 2.3 nF and C_c = 4.7 nF, is obtained, as shown in Fig. 13. The phase margin calculated from the Bode plot is 36.7 °, and the gain-bandwidth-product (GBW) is 2.8 kHz.

The transient behavior of the TIA with the gain-boosted op-amp in response to a sinusoidal input current with an amplitude of ±12.5 μA, offset by 75 μA, and frequencies ranging from 100 to 500 Hz has also been measured. The circuit behaves as expected for frequencies up to 300 Hz, with a transimpedance of 16.86 kΩ. The transient response of the circuit for a frequency of 100 Hz is shown in Fig. 14(a). At frequencies higher than 300 Hz, the op-amp response no longer follows the frequency of the input current, resulting in charging and discharging of the capacitance at the input node, which leads to the distortion of the time dependence of the output voltage at a frequency of 500 Hz seen in Fig. 14(b).

B. CG-Based TIA

The GB CG TIA topology, first published in [40], is shown in Fig. 15. The structure of the CB CG TIA topology consists of two main parts: the input stage (gray rectangle) and the implementation of the resistor (three yellow rectangles). As described in [40], a CG input stage is used for the

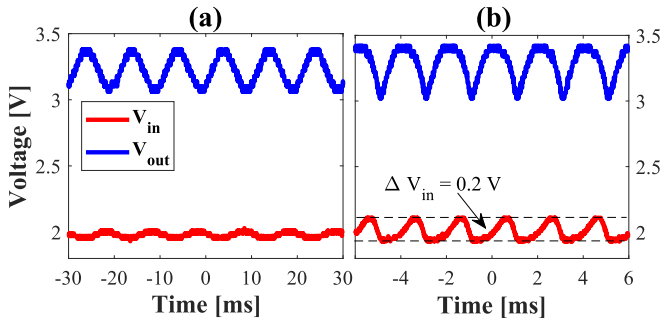


Fig. 14. Measured transient behavior of the input and output voltages of the closed-loop gain-boosted op-amp-based TIA for a sinusoidal input current with an amplitude of ±12.5 μA, a dc offset of 75 μA, and a frequency of (a) 100 and (b) 500 Hz.

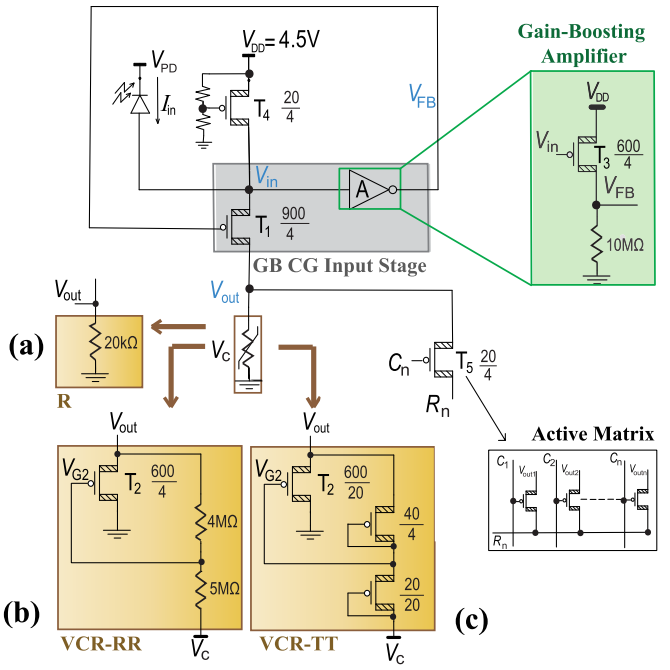


Fig. 15. Circuit schematic of a GB CG TIA with either (a) integrated passive resistor (R) with an ohmic resistance of 20 kΩ, (b) VCR with a voltage divider implemented using passive resistors (VCR-RR), and (c) VCR with a voltage divider implemented using diode-connected transistors (VCR-TT).

input current, taking advantage of its small input impedance ($r_{\text{in}} = 1/gm_1$). A gain-boosting feedback circuit is connected to the gate of transistor T_1 in order to further reduce the input impedance ($r_{\text{in}} = 1/(A \cdot gm_1)$) and, thus, stabilize the voltage at the input node (V_{in}) at a fixed value irrespective of any changes in input current. The transistor T_4 is biased to set V_{in} at 3.5 V when the current through T_4 is equal to 0.02 μA.

The impedance needed for the linear current-to-voltage conversion is implemented in three different ways: 1) with an integrated passive thin-film carbon resistor (R), as shown in Fig. 15(a); 2) with a voltage-controlled resistor (VCR) with a voltage divider based on passive resistors (VCR-RR) [see Fig. 15(b)]; and 3) with a VCR with a voltage divider based on diode-connected TFTs (VCR-TT) [see Fig. 15(c)]. The concept of the simple and highly linear VCR is explained

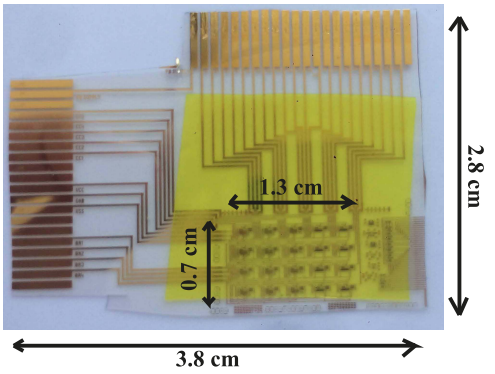


Fig. 16. Photograph of an array of GB CG TIAs fabricated on a flexible plastic substrate using organic TFTs and thin-film carbon resistors. Two columns consist of TIA cells with R according to Fig. 15(a), one column consists of TIA cells with VCR-RR according to Fig. 15(b), and two columns consist of TIA cells with VCR-TT according to Fig. 15(c).

in detail in [40], where the gate of the transistor T_2, which operates in the triode region, is controlled by a voltage divider from the source node of T_2. The value of the transimpedance can be estimated according to the following equation:

$$VCR = \frac{L_2}{\mu_{\text{eff}} \cdot C_{\text{diel}} \cdot W_2 \cdot (V_{\text{th}} - V_c(1 - \text{FBF}))} \tag{10}$$

where FBF is the feedback factor from the voltage divider. The VCR achieves a linear resistance of 20 kΩ for a control voltage $V_c = -5.5$ V.

A photograph of the fabricated GB CG TIA array is shown in Fig. 16. Each of the two leftmost columns contains four TIA cells with VCR-TT according to Fig. 15(c), the third column contains four TIA cells with VCR-RR according to Fig. 15(b), and the two rightmost columns contain four TIA cells each with R according to Fig. 15(a). The 20 TIA cells are arranged in a 4 × 5 active matrix in order to reduce the number of connections from 20 to 9. This is realized by adding an additional switch transistor T_5 at the output node of each TIA, which is selectively addressed by the column select signal (C_n) to transfer the output voltage to the row signal (R_n), as shown in Fig. 15. The time interval between column selection and the start of the measurement is several hundred milliseconds, i.e., sufficiently long to not impact the results of the measurements. However, according to [42], the sum of the rise and fall times of a TFT with dimensions similar to that of T_5 is about 400 μs, which suggests a maximum frame rate of about 500 frames/s.

For a supply voltage (V_{DD}) of 4.5 V, a control voltage (Vc) of −5.5 V, and under dark condition, the feedback gain-boosting amplifier draws an average current of 0.2 μA, and the average current flowing through the feedback branch of the VCR is 0.6 μA. Therefore, the overall measured power consumption in the dark is 4.2 μW for each of the TIA cells with VCR-RR or VCR-TT (12 cells) and 0.9 μW for each of the TIA cells with a passive resistor R (eight cells). This results in a total power consumption in the dark of 57.6 μW for the complete array.

Fig. 17(a) shows the measured and simulated voltages present at the circuit nodes V_{in}, V_{out}, and V_{FB} of a GB CG TIA with a VCR-TT for a sweep of the input current from

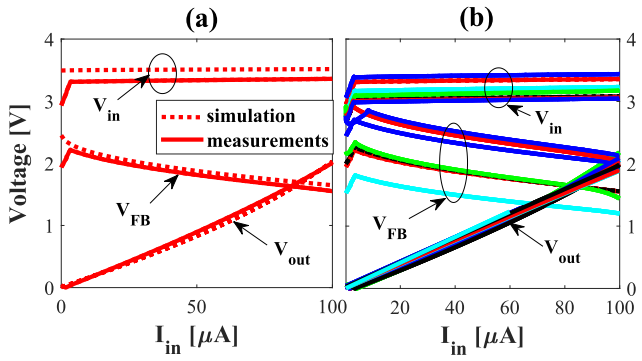


Fig. 17. (a) Measured (continuous lines) and simulated (dotted lines) voltages present at the circuit nodes V_{out}, V_{FB}, and V_{in} of the GB CG TIA with a VCR-TT. (b) Results of measurements performed on several such GB CG TIA circuits [35] (2019, IEEE).

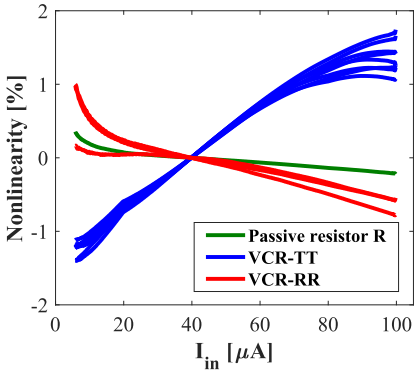


Fig. 18. Transimpedance nonlinearity of the 20 GB CG TIAs shown in Fig. 16, extracted from their measured voltage–current characteristics.

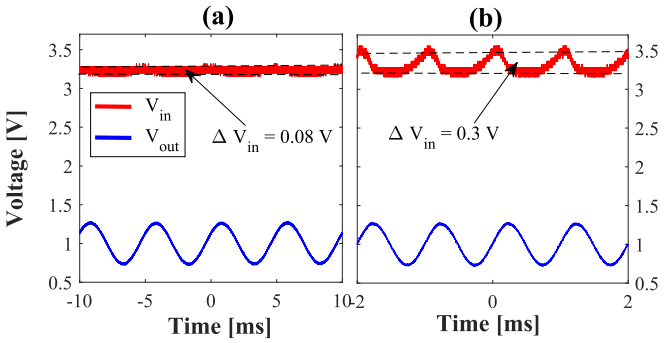


Fig. 19. Measured transient behavior of the input and the output voltages of a GB CG TIA with a VCR-TT in response to a sinusoidal input current with an amplitude of ±12.5 μA, a dc offset of 50 μA, and frequencies of (a) 200 Hz and (b) 1 kHz.

0 to 100 μA. The measured voltage–current characteristics of several TIAs are plotted in Fig. 17(b) that shows that the simulation results are approximately consistent with the average of the measurement results. Although V_{in} and V_{FB} show a spread of characteristics due to unavoidable process variations, the relation between the input current (I_{in}) and the output voltage (V_{out}) is nearly identical for all cells, which confirms the robustness of the topology.

To estimate how the transimpedance (*VCR*) of the VCR is affected by the variations in the TFT parameters (effective carrier mobility and threshold voltage), the following equation can be derived from (10):

$$\frac{\Delta VCR}{VCR} = -\frac{\Delta \mu_{\text{eff}}}{\mu_{\text{eff}}} - \frac{\Delta V_{\text{th}}}{V_{\text{th}} - V_c(1 - \text{FBF})}. \tag{11}$$

For the parameter variations mentioned in Section III-A (±5% for the effective carrier mobility and ±1.2% for the threshold voltage), the transimpedance *VCR* can vary by up to ±6.8%. For comparison, the transimpedance of the op-amp-based TIA shown in Fig. 5 can vary by up to ±11.7%.

Fig. 17(b) indicates that the circuits have an input impedance of 520 Ω, which results in a maximum light-to-current linearity error of no more than ±0.64% for the PDs used in this article for each individual cell. However, since the input voltage of the TIAs varies by about 0.5 V due to circuit-to-circuit process variations, the mismatch error of the final output voltage reading among the sensor cells is ±7.7%.

The transimpedance linearity of each of the 20 circuits shown in Fig. 16 is plotted in Fig. 18. The GB CG TIA circuits with R show a nonlinearity of no more than ±0.3%. The circuits with VCR-RR show a nonlinearity of ±1.0%. Finally, the VCR-TT circuits have a nonlinearity of ±2.0%. Therefore, using the resistor R has the advantages of achieving a smaller occupied area, lower power consumption, and better linearity. On the other hand, VCRs provide greater robustness against parameter nonuniformity and enhanced capability of tuning, which is important when the technology suffers from significant device-to-device and/or substrate-to-substrate variations. An additional advantage of the VCR-TT is that it does not require the fabrication and integration of resistors, which, in thin-film electronics, are often more difficult to implement than transistors.

The transient response of a GB CG TIA with a VCR-TT to a sinusoidal input current with an amplitude of ±12.5 μA, a dc offset of 50 μA, and frequencies of 200 Hz and 1 kHz is shown in Fig. 19. The reason that this circuit is considered for this analysis is that it shows the longest response time in comparison with the other two impedance topologies. As can be seen, the output voltage shows excellent linearity for all frequencies up to 1 kHz with a transimpedance of 20 kΩ.

At high frequencies (1 kHz), a distortion of the time dependence of the input voltage similar to that of the op-amp-based TIA in Fig. 14(b) is observed, which is due to the fact that the gain-boosting feedback circuit no longer follows the frequency of the input current, resulting in charging and discharging of the capacitance at the input node. However, unlike in the op-amp-based TIA in Fig. 14, in the GB CG TIA in Fig. 19, this input-voltage distortion does not have any influence on the output voltage V_{out}, which can be seen to be perfectly linear with respect to I_{in}. This beneficial characteristic is the result of the fact that in the GB CG TIA, the input- and output-voltage paths are separate, which eliminates the dependence of the linearity of the output voltage on the linearity of the input voltage. The output-voltage linearity of our GB CG TIA is, thus, limited only by the output resistance of the PD. A PD with an output resistance of 10 GΩ in the dark (such as the commercially available PD SFH 213 [43]), which is able to tolerate large variations in the virtual-ground voltage of the TIA (V_{in}), would result in an output voltage perfectly linear for frequencies up to 21 kHz.

TABLE IV

COMPARISON OF THE CHARACTERISTICS OF THE OP-AMP-BASED AND THE GB CG TIA PRESENTED IN SECTIONS III-A AND III-B WITH ORGANIC-TFT-BASED OP-AMPS AND TIAS REPORTED IN THE LITERATURE

	Maiellaro et al., TCAS I, 2014 [8]	Garripoli et al., JETCAS, 2016 [44]	Chen et al., JEDS, 2018 [45]	Seifaei et al., A-SSCC, 2018 [46]	This work op-amp TIA	This work GB CG TIA
Fabrication technology	plastic substrate, inkjet printing, laser ablation (complementary organic TFTs)	plastic substrate, sputtering, wet-etching (n-channel a-IGZO TFTs)	glass substrate, sputtering, wet-etching (n-channel IZO TFTs)	plastic substrate, vacuum-deposition, stencil lithography (p-channel organic TFTs)	plastic substrate, vacuum-deposition, stencil lithography (p-channel organic TFTs)	plastic substrate, vacuum-deposition, stencil lithography (p-channel organic TFTs)
Minimum L_{ch} [µm]	20	15	10	20	4	4
Design base	Classical 2-stage op-amp TIA	Op-amp with gain boosting techniques	Op-amp with gain boosting techniques	1-stage op-amp	Gain-boosted op-amp TIA	Common-gate TIA
Op-amp DC gain [dB]	54	30	29.54	26.1	41.3	-
Op-amp GBW [Hz]	57 *	5500	180000	900	2800	-
-3dB frequency [Hz]	NA	150	9330	50	130	21000 **
Phase margin with comp.	60^o *	NA	21.5^o	NA	36.7^o	-
Step settling time [ms]	60	NA	NA	NA	1.4	0.5
Transimpedance realization	External on PCB	-	-	-	Integrated	Integrated
Transimpedance Tunability	No	-	-	-	No	Yes
Transimpedance nonlinearity	NA	-	-	-	±0.45 %	±0.3 - ±1 % - ±2 %
ΔV/ΔI range	2 V/3 µA	-	-	-	1.6 V/100 µA	2 V/100 µA
External comp. components	Yes	-	-	-	Yes	No
Circuit area [mm^2]	300	0.87 ***	1.105	5	1.87	1.25 - 1.6 - 1.8
Power consumption [µW]	360	0.4	5070	1.4	7.2	0.9 - 4.2 - 4.2
Voltage supply [V]	40	±10	15	5	4.5	4.5

* Simulated values.
** For a detector with an output resistance as high as 10 GΩ.
*** Calculated from Fig. 9.

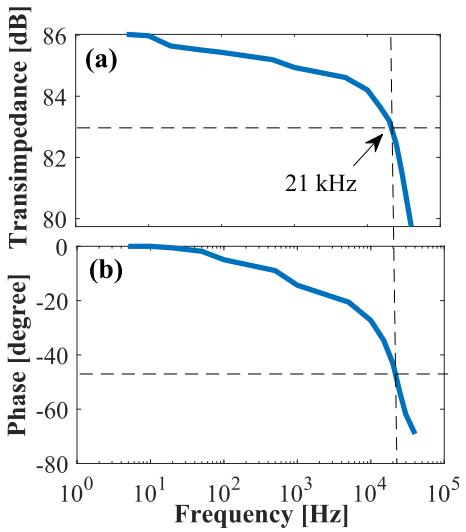


Fig. 20. Bode plot of the transimpedance of the GB CG TIA. (a) Transimpedance as a function of frequency. (b) Phase as a function of frequency.

The frequency dependence of the transimpedance of the GB CG TIA on the input signal frequency is shown in Fig. 20. For the organic PDs employed in this article (output resistance of 360 kΩ in the dark), the fluctuations of 0.3 V observed at the input node at a frequency of 1 kHz [see Fig. 19(b)] will result in additional fluctuations of I_{in} as well, producing an output-voltage peak-to-peak error of −33.1%.

The fast Fourier transform (FFT) of the output-voltage signal (V_{out}) from Fig. 19(a) results in the power spectral density (PSD) shown in Fig. 21. By excluding the signal peak, the in-band noise (IBN) can be calculated by integrating the PSD over the bandwidth frequency. This results in an IBN of 80 nArms within a bandwidth of 2 kHz, which is equivalent to a resolution of 9.8 bit, assuming a full scale of 100 μA. For this resolution, the minimum resolved illumination is as low as 12 klx.

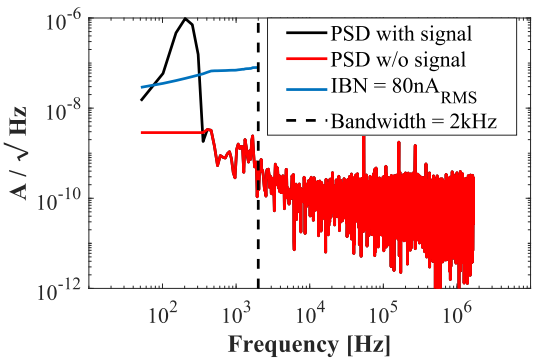


Fig. 21. PSD of the output voltage (V_{out}) of the GB CG TIA from Fig. 19(a) showing the IBN of approximately 80 nArms within a bandwidth of 2 kHz for a full scale of 100 μA.

C. CG Versus Op-Amp TIA

A comparison of the performance characteristics of the op-amp-based and the GB CG TIA presented in Sections III-A and III-B with the organic-TFT-based op-amps and TIAs reported in [8] and [44]–[46] is provided in Table IV. Although the op-amp-based TIA compares quite favorably,

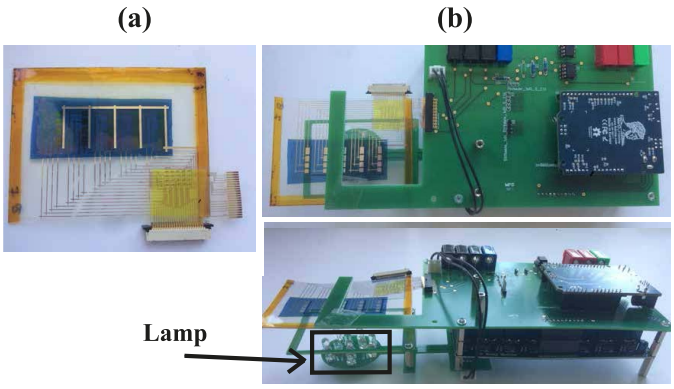


Fig. 22. Imaging system. (a) Photograph showing the integration of the two foils containing the OPD array (dark blue) and the organic-TFT-based TIA readout array (covered with yellow foil to shield the TFTs from illumination). (b) Photographs showing the integration of the flexible PD/TIA stack with an LED lamp and a printed circuit board containing power supplies and a microcontroller to control the LED lamp and process the TIA data.

especially in terms of dc gain, bandwidth, and circuit area, it has a number of inherent disadvantages that will ultimately limit its usefulness for the imaging system considered in Section IV. The first drawback is that despite the large dc gain produced by the gain-boosting approach and the use of integrated passive carbon resistors, the overall transimpedance suffers from a slight variation depending on the input current delivered by the PD [nonlinearity of ±0.45%, see Fig. 10(b)], which will add to the overall nonlinearity of the sensor. The second drawback is that the use of a differential stage leads to mismatch problems not only from cell to cell but also within the same cell due to the device-to-device variations inherent to organic TFTs. This adds to the overall nonlinearity of the system. The third drawback of the op-amp-based TIA is that to ensure stability, frequency-compensation capacitors need to be added and tuned externally for each cell, which will significantly complicate the system. In contrast, the GB CG TIA topology provides simpler implementation with lower power consumption and shorter response time in addition to allowing the TIA to be tuned. Finally, the GB CG TIA offers a higher level of robustness against parameter variations. We, therefore, chose the GB CG TIA topology for the realization of the imaging system discussed in Section IV.

IV. Imaging System

The foil with the zero-biased OPD array is attached to the organic-TFT-based active-matrix GB CG TIA readout array, as shown in Fig. 22(a). The foil with the TIA array is then connected through a flat-cable socket to a custom-built printed-circuit board containing power supplies and a microcontroller, as shown in Fig. 22(b). Since the semiconductor employed in the organic TFTs (DNTT) is sensitive to visible and ultraviolet light, as discussed in detail in [47], the TIA array is covered with yellow foil to shield the TFTs from illumination.

To test the imaging system, the PDs were illuminated from a lamp consisting of 12 high-power light-emitting diodes (LED EL5-36000 WS) whose illuminance is linearly controlled from 0 to 10 klx by applying a dc voltage between 0 and 1.2 V. The output voltages produced by the TIA array were read and

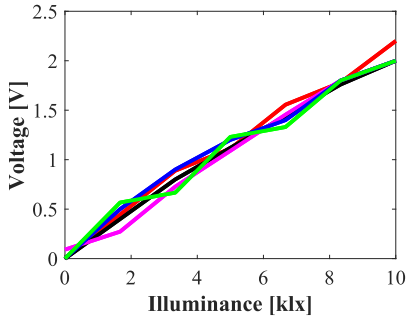


Fig. 23. Measured output voltages of five PD/TIA cells of the imaging system as a function of illuminance.

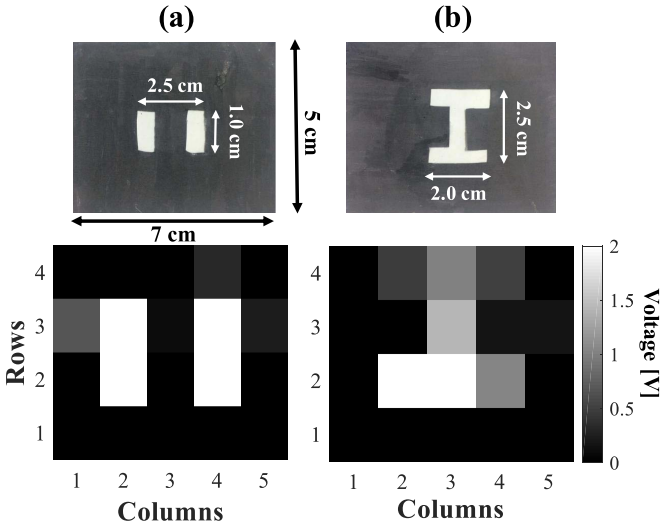


Fig. 24. Photographs of two shadow masks with transparent openings in the shape of (a) two vertical bars and (b) letter "I" employed to test the imaging system (top row) and 4 × 5 pixel gray-scale images representing the output voltages of the PD/TIA array in response to illumination with an illuminance of 10 klx through the shadow masks (bottom row).

interpreted into a 4 × 5 pixel gray-scale image displayed on a computer monitor by a Nero Arduino module in order to visualize the functionality of the imaging system. A CM was applied to account for the mismatch errors arising from the circuit-to-circuit variations (0.5 V) present at the input nodes of the TIAs, as seen in Fig. 17(b), and from the device-to-device responsivity variations of the OPD cells. One of the four rows was blocked because of non-functional PDs

$$\mathrm{CM} = \begin{bmatrix} 2.5 & 1.8 & 3.3 & 0.8 & 4.0 \\ 0.7 & 4.4 & 2.8 & 0.9 & 1.2 \\ 2.2 & 0.8 & 3.0 & 4.9 & 2.0 \\ 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \end{bmatrix}.$$

In Fig. 23, the measured output voltages from five PD/TIA cells are plotted as a function of illuminance, demonstrating the linear conversion of the light illuminance. The maximum measured illuminance-to-voltage nonlinearity for these five PD/TIA cells is 19%. Generically, the overall linearity error for one cell can arise from the nonlinearity of the PD responsivity, the nonlinearity of the TIA circuit, and the error due to the output resistance of the PD and/or the input resistance of the TIA. Considering the small value of the CG TIA nonlinearity

(maximum 2%) and its small input impedance (which results in a maximum error of 0.64%), the overall nonlinearity of the system is mainly attributed to the contribution of the nonlinearity of the PDs responsivity, as shown in Fig. 2(b).

In another test of the imaging system, an opaque shadow mask with transparent openings in the shape of either two vertical bars or the letter "I" was placed in front of the PD array. The results are shown in Fig. 24, confirming the ability of the system to resolve different illumination patterns. The gray-scale variations observed in the images are caused by variations in the illuminance and the angle of incidence of the light passing through the openings of the shadow masks.

V. Conclusion

In this article, a 57.6-μW mechanically flexible active-matrix imaging system based on OPDs and organic-TFT-based TIAs fabricated on plastic substrates has been proposed, simulated, fabricated, and characterized. The imaging system is composed of 4×5 arrays of OPDs and GB CG TIAs. The encapsulated PDs have an area of 0.1 cm^2, an average illuminance-to-current conversion ratio of 10 μA/klx, and an output resistance of 180 kΩ at an illuminance of 2 klx. We have shown the advantages of implementing the TIAs in a gain-boosted CG rather than op-amp-based topology in terms of process complexity, linearity, stability, response time, and power consumption. A complete imaging system comprising a PD array, a readout TIA array, and an evaluation board has been assembled and tested in ambient air by converting the output voltages of the TIA array into a gray-scale image.

Acknowledgment

The authors acknowledge Kazuo Takimiya (RIKEN Center for Emergent Matter Science, Wako, Saitama, Japan) and Koichi Ikeda, Yuichi Sadamitsu, and Satoru Inoue (Nippon Kayaku, Tokyo, Japan) for providing the organic semiconductor DPh-DNTT. Also, they thank Linda Moschallski, Birger Zimmermann, and Hans-Frieder Schleiermacher for the design and fabrication of the PD devices.

References

[1] B. Peng, X. Ren, Z. Wang, X. Wang, R. C. Roberts, and P. K. L. Chan, "High performance organic transistor active-matrix driver developed on paper substrate," *Sci. Rep.*, vol. 4, Dec. 2014, Art. no. 6430, doi: 10.1038/srep06430.

[2] T. Yokota *et al.*, "Sheet-type flexible organic active matrix amplifier system using pseudo-CMOS circuits with floating-gate structure," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3434–3441, Dec. 2012, doi: 10.1109/TED.2012.2220853.

[3] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, and T. Sakurai, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications," *Proc. Nat. Acad. Sci. USA*, vol. 101, no. 27, pp. 9966–9970, Jul. 2004, doi: 10.1073/pnas.0401918101.

[4] S. C. B. Mannsfeld *et al.*, "Highly sensitive flexible pressure sensors with microstructured rubber dielectric layers," *Nature Mater.*, vol. 9, no. 10, pp. 859–864, Oct. 2010, doi: 10.1038/nmat2834.

[5] T. Moy, L. Huang, W. Rieutort-Louis, S. Wagner, J. C. Sturm, and N. Verma, "16.4 a flexible EEG acquisition and biomarker extraction system based on thin-film electronics," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 294–295, doi: 10.1109/ISSCC.2016.7418023.

[6] C. Bartic and G. Borghs, "Organic thin-film transistors as transducers for (bio) analytical applications," *Anal. Bioanal. Chem.*, vol. 384, no. 2, pp. 354–365, Dec. 2005, doi: 10.1007/s00216-005-0031-8.

[7] G. Scarpa, A.-L. Idzko, A. Yadav, E. Martin, and S. Thalhammer, "Toward cheap disposable sensing devices for biological assays," *IEEE Trans. Nanotechnol.*, vol. 9, no. 5, pp. 527–532, Sep. 2010, doi: 10.1109/TNANO.2010.2060493.

[8] G. Maiellaro *et al.*, "Ambient light organic sensor in a printed complementary organic TFT technology on flexible plastic foil," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 4, pp. 1036–1043, Apr. 2014, doi: 10.1109/TCSI.2013.2286031.

[9] J. W. Jeong *et al.*, "The emission properties of integrated organic light emitting diodes with organic photo sensor for emotional lighting applications," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 348–350, Mar. 2011, doi: 10.1109/LED.2010.2099099.

[10] F. De Roose *et al.*, "16.5 a flexible thin-film pixel array with a charge-to-current gain of 59 μA/pC and 0.33% nonlinearity and a cost effective readout circuit for large-area X-ray imaging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 296–297, doi: 10.1109/ISSCC.2016.7418024.

[11] K. S. Karim, A. Nathan, and J. A. Rowlands, "Amorphous silicon active pixel sensor readout circuit for digital imaging," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 200–208, Jan. 2003, doi: 10.1109/TED.2002.806968.

[12] S. Tedde, E. S. Zaus, J. Furst, D. Henseler, and P. Lugli, "Active pixel concept combined with organic photodiode for imaging devices," *IEEE Electron Device Lett.*, vol. 28, no. 10, pp. 893–895, Oct. 2007, doi: 10.1109/LED.2007.905425.

[13] L. Bärgi, R. Pfeiffer, M. Mücklich, P. Metzler, M. Kiy, and C. Winnewisser, "Optical proximity and touch sensors based on monolithically integrated polymer photodiodes and polymer LEDs," *Organic Electron.*, vol. 7, no. 2, pp. 114–120, Apr. 2006, doi: 10.1016/j.orgel.2005.12.002.

[14] T. Someya *et al.*, "Integration of organic FETs with organic photodiodes for a large area, flexible, and lightweight sheet image scanners," *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp. 2502–2511, Nov. 2005, doi: 10.1109/TED.2005.857935.

[15] I. Nausieda, K. Ryu, I. Kymissis, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "An organic imager for flexible large area electronics," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 72–73, doi: 10.1109/ISSCC.2007.373593.

[16] S. Aihara *et al.*, "Stacked image sensor with Green- and red-sensitive organic photoconductive films applying zinc oxide thin-film transistors to a signal readout circuit," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2570–2576, Nov. 2009, doi: 10.1109/TED.2009.2030607.

[17] E. Kraft *et al.*, "Counting and integrating readout for direct conversion X-ray imaging: Concept, realization and first prototype measurements," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 2, pp. 383–390, Apr. 2007, doi: 10.1109/TNS.2007.891571.

[18] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994, doi: 10.1109/16.337449.

[19] F. Schwierz and J. J. Liou, "RF transistors: Recent developments and roadmap toward terahertz applications," *Solid-State Electron.*, vol. 51, no. 8, pp. 1079–1091, Aug. 2007, doi: 10.1016/j.sse.2007.05.020.

[20] B. Sell *et al.*, "22FFL: A high performance and ultra low power FinFET technology for mobile and RF applications," in *IEDM Tech. Dig.*, Dec. 2017, p. 29, doi: 10.1109/IEDM.2017.8268475.

[21] K. H. Cherenack, B. Hekmatshoar, J. C. Sturm, and S. Wagner, "Self-aligned amorphous silicon thin-film transistors fabricated on clear plastic at 300 °C," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2381–2389, Oct. 2010, doi: 10.1109/TED.2010.2056132.

[22] L. Han, P. Mandlik, K. H. Cherenack, and S. Wagner, "Amorphous silicon thin-film transistors with field-effect mobilities of 2 cm2/V s for electrons and 0.1 cm2/V s for holes," *Appl. Phys. Lett.*, vol. 94, no. 16, Apr. 2009, Art. no. 162105, doi: 10.1063/1.3119636.

[23] Y. Kubota, T. Matsumoto, H. Tsuji, N. Suzuki, S. Imai, and H. Kobayashi, "1.5-V-Operation ultralow power circuit of poly-Si TFTs fabricated using the NAOS method," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 385–392, Feb. 2012.

[24] J. Lee *et al.*, "5.8-inch QHD flexible AMOLED display with enhanced bendability of LTPS TFTs," *J. Soc. Inf. Display*, vol. 26, no. 4, pp. 200–207, Apr. 2018, doi: 10.1002/jsid.655.

[25] T.-C. Chang *et al.*, "Flexible low-temperature polycrystalline silicon thin-film transistors," *Mater. Today Adv.*, vol. 5, Mar. 2020, Art. no. 100040, doi: 10.1016/j.mtadv.2019.100040.

[26] N. Munzenrieder, L. Petti, C. Zysset, T. Kinkeldei, G. A. Salvatore, and G. Troster, "Flexible self-aligned amorphous InGaZnO thin-film transistors with submicrometer channel length and a transit frequency of 135 MHz," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2815–2820, Sep. 2013, doi: 10.1109/TED.2013.2274575.

[27] R. A. Lujan and R. A. Street, "Flexible X-ray detector array fabricated with oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 688–690, May 2012, doi: 10.1109/LED.2012.2188825.

[28] S. Abdinia *et al.*, "Organic CMOS line drivers on foil," *J. Display Technol.*, vol. 11, no. 6, pp. 564–569, Jun. 2015, doi: 10.1109/DT.2015.2421344.

[29] A. Yamamura *et al.*, "High–speed organic single crystal transistor responding to very high frequency band," *Adv. Funct. Mater.*, vol. 30, no. 11, Mar. 2020, Art. no. 1909501, doi: 10.1002/adfm.201909501.

[30] U. Zschieschang *et al.*, "Roadmap to gigahertz organic transistors," *Adv. Funct. Mater.*, vol. 30, no. 20, May 2020, Art. no. 1903812, doi: 10.1002/adfm.201903812.

[31] G. Dennler, M. C. Scharber, and C. J. Brabec, "Polymer-fullerene bulk-heterojunction solar cells," *Adv. Mater.*, vol. 21, no. 13, pp. 1323–1338, Apr. 2009, doi: 10.1002/adma.200801283.

[32] C. Deibel and V. Dyakonov, "Polymer–fullerene bulk heterojunction solar cells," *Rep. Prog. Phys.*, vol. 73, no. 9, Sep. 2010, Art. no. 096401, doi: 10.1088/0034-4885/73/9/096401.

[33] J. Nelson, "Polymer:fullerene bulk heterojunction solar cells," *Mater. Today*, vol. 14, no. 10, pp. 462–470, 2011, doi: 10.1016/S1369-7021(11)70210-3.

[34] U. Würfel, D. Neher, A. Spies, and S. Albrecht, "Impact of charge transport on current–voltage characteristics and power-conversion efficiency of organic solar cells," *Nature Commun.*, vol. 6, no. 1, p. 6951, Nov. 2015, doi: 10.1038/ncomms7951.

[35] S. Elsaegh, U. Zschieschang, J. W. Borchert, H. Klauk, H. Zappe, and Y. Manoli, "Compact DC modeling of organic thin-film transistors including their parasitic non-linear contact effects based on a novel extraction method," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4907–4914, Nov. 2019, doi: 10.1109/TED.2019.2941438.

[36] U. Kraft *et al.*, "Detailed analysis and contact properties of low-voltage organic thin-film transistors based on dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene (DNTT) and its didecyl and diphenyl derivatives," *Organic Electron.*, vol. 35, pp. 33–40, Aug. 2016, doi: 10.1016/j.orgel.2016.04.038.

[37] H. Ryu, D. Kälblein, O. G. Schmidt, and H. Klauk, "Unipolar sequential circuits based on Individual-Carbon-Nanotube transistors and thin-film carbon resistors," *ACS Nano*, vol. 5, no. 9, pp. 7525–7531, Sep. 2011, doi: 10.1021/nn202486v.

[38] T. Zaki *et al.*, "A 3.3 v 6-Bit 100 kS/s current-steering Digital-to-Analog converter using organic P-Type thin-film transistors on glass," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 292–300, Jan. 2012, doi: 10.1109/JSSC.2011.2170639.

[39] M. Ramuz, L. Bärgi, C. Winnewisser, and P. Seitz, "High sensitivity organic photodiodes with low dark currents and increased lifetimes," *Organic Electron.*, vol. 9, no. 3, pp. 369–376, Jun. 2008, doi: 10.1016/j.orgel.2008.01.007.

[40] S. Elsaegh, H. Zappe, Y. Manoli, Y. Manoli, H. Klauk, and U. Zschieschang, "A 1.6μW tunable organic transimpedance amplifier for photodetector applications based on gain-boosted common-gate input stage and voltage-controlled resistor with $\pm$0.5% nonlinearity," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf.*, Sep. 2017, pp. 75–78, doi: 10.1109/ESSCIRC.2017.8094529.

[41] N. S. Nise, *Control Systems Engineering*. Hoboken, NJ, USA: Wiley, 2007.

[42] M. Elsobky *et al.*, "A digital library for a flexible low-voltage organic thin-film transistor technology," *Organic Electron.*, vol. 50, pp. 491–498, Nov. 2017, doi: 10.1016/j.orgel.2017.08.028.

[43] *SFH 213 Silicon Pin Photodiode*, OSRAM, Munich, Germany, 2015.

[44] C. Garripoli *et al.*, "Analogue frontend amplifiers for bio-potential measurements manufactured with a-IGZO TFTs on flexible substrate," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 7, no. 1, pp. 60–70, Mar. 2017, doi: 10.1109/JETCAS.2016.2616723.

[45] Z.-J. Chen *et al.*, "A new high-gain operational amplifier using transconductance-enhancement topology integrated with metal oxide TFTs," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 111–117, 2019, doi: 10.1109/JEDS.2018.2883585.

[46] M. Seifaei *et al.*, "Stable, self-biased and high-gain organic amplifiers with reduced parameter variation effect," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2018, pp. 119–122, doi: 10.1109/ASSCC.2018.8579293.

[47] J. Milvich *et al.*, "Flexible low-voltage organic phototransistors based on air-stable dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene (DNTT)," *Organic Electron.*, vol. 20, pp. 63–68, May 2015, doi: 10.1016/j.orgel.2015.02.007.

Samar Elsaegh received the B.Sc. degree in electronics and communication engineering from Ain Shams University, Cairo, Egypt, in 2008, and the M.Sc. degree in microsystems engineering from IMTEK, University of Freiburg, Freiburg, Germany, in 2012, where she is currently pursuing the Ph.D. degree with the Fritz Hüttinger Chair of Microelectronics in collaboration with the Gisela and Erwin Sick Chair of Micro-optics.

Her main research interest includes analog and analog-to-digital converters circuit design based on organic thin-film transistors for photodetector applications.

Clemens Veit received the Engineering degree in applied physics from the University of Applied Science Ravensburg-Weingarten, Weingarten, Germany, in 2008.

Since 2009, he has been with the Fraunhofer Institute for Solar Energy Systems (ISE), Freiburg, Germany, in research and development of organic photovoltaics. He has a very broad research interest in all the steps from small lab scale cells to large roll to roll processed modules.

Ute Zschieschang received the Dipl.-Ing. degree in mechanical engineering from the Mittweida University of Applied Sciences (FH), Mittweida, Germany, in 2000, and the Ph.D. degree in chemistry from Technical University Bergakademie Freiberg, Freiberg, Germany, in 2006.

Since 2005, she has been a Scientist with Organic Electronics Group, Max Planck Institute for Solid State Research, Stuttgart, Germany.

Mohammad Amayreh was born in Dora, Palestine, in 1987. He received the B.Sc. degree (Hons.) in mechatronics engineering from Palestine Polytechnic University, Hebron, Palestine, in 2010, and the M.Sc. and Ph.D. degrees in microelectronics engineering from the University of Freiburg, Freiburg, Germany, in 2014 and 2019, respectively.

He is currently a Researcher at the Hahn-Schickard-Gesellschaft für angewandte Forschung, Freiburg. His research interests include ultralow noise current readout based on CT DSMs for biological nanopores.

Florian Letzkus received the master's degree in physics from the University of Tübingen, Tübingen, Germany, in 1996, and the Ph.D. degree from the University of Stuttgart, Stuttgart, Germany, in 2003.

He is currently heading the Nanoprocess Department IMS CHIPS, Stuttgart.

Holger Sailer received the Dipl.-Phys. and the Ph.D. degrees in physics from the University of Tübingen, Tübingen, Germany, in 2000 and 2007, respectively, for work on high-resolution electron-beam resists.

In 2004, he joined IMS CHIPS, Stuttgart, Germany, where he manages projects related to e beam, i-line, and laser-lithography. Since 2017, he has been the Head of the Lithography Department, IMS CHIPS.

Michael Jurisch received the Dipl.-Ing. degree in electrical engineering from the University of Applied Science, Zweibrücken, Germany, in 2007, and the Ph.D. degree in mechanical engineering from the University of Stuttgart, Stuttgart, Germany, in 2017.

He has been with IMS CHIPS, Stuttgart, since 2007, where he is responsible for silicon etching and MEMS components' assembly.

Joachim N. Burghartz (Fellow, IEEE) received the Dipl.-Ing. degree in electrical engineering from RWTH Aachen, Aachen, Germany, in 1982, and the Ph.D. degree in electrical engineering from the University of Stuttgart, Stuttgart, Germany, in 1987.

He is the Director of IMS CHIPS, Stuttgart, and a Full Professor with the University of Stuttgart.

Uli Würfel received the Ph.D. degree in physics from the University of Freiburg, Freiburg, Germany, in 2006.

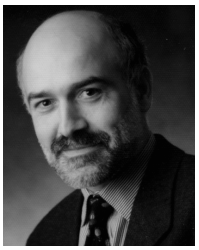
Since 2009, he has been the Head of the Department "Organic and Perovskite Photovoltaics," Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, and the group "Organic and Perovskite Solar Cells," Freiburg Materials Research Center FMF, University of Freiburg. His work is mainly dedicated to the characterization and modeling of organic and perovskite solar cells, their upscaling, and their long-term stability. He has coauthored 70 scientific articles on solar cells. His research interests include the general working principles and theoretical modeling of solar cells.

Hagen Klauk received the Dipl.-Ing. degree in electrical engineering from the Chemnitz University of Technology, Chemnitz, Germany, in 1995, and the Ph.D. degree in electrical engineering from Pennsylvania State University, University Park, PA, USA, in 1999.

In 2000, he joined the Polymer Electronics Group, Infineon Technologies, Erlangen, Germany. Since 2005, he has been the Head of the Organic Electronics Group, Max Planck Institute for Solid State Research, Stuttgart, Germany.

Hans Zappe was born in Paris and raised in New York. He received the bachelor's and master's degrees from MIT, Cambridge, MA, USA, in 1983 and the Ph.D. degree from the University of California at Berkeley, Berkeley, CA, USA, in 1989, all in electrical engineering.

He has worked at IBM, Essex, VT, USA, the Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany, and the Centre Suisse d'Electronique et de Microtechnique, Switzerland. He joined the Department of Microsystems Engineering, University of Freiburg, Freiburg, Germany, in 2000.



Yiannos Manoli (Life Fellow, IEEE) was born in Famagusta, Cyprus, in 1954. He received the B.A. degree *(summa cum laude)* in physics and mathematics from Lawrence University, Appleton, WI, USA, in 1978, the M.S. degree in electrical engineering and computer science from the University of California at Berkeley, Berkeley, CA, USA, in 1980, both on a Fulbright Scholarship, and the Dr.-Ing. degree in electrical engineering from Gerhard Mercator University, Duisburg, Germany, in 1987.

From 1980 to 1984, he was a Research Assistant with the University of Dortmund, Dortmund, Germany, in the field of A/D and D/A converters. In 1985, he joined the newly founded Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany, where he established a design group working on mixed-signal CMOS circuits especially for monolithic integrated sensors and application-specific microcontrollers. From 1996 to 2001, he held the Chair of Microelectronics as a Full Professor with the Department of Electrical Engineering, University of Saarland, Saarbrücken, Germany. In 2001, he joined the Department of Microsystems Engineering (IMTEK), Faculty of Engineering, University of Freiburg, Freiburg, Germany, where he established the Chair of Microelectronics. In memory of the founder of today's Trumpf Hüttinger GmbH, this chair was endowed by the Fritz Hüttinger Foundation in 2010 and has since carried the name "Fritz Huttinger Chair of Microelectronics." From 2008 to 2015, he served as the Associate Dean and the Dean of the Faculty of Engineering. Since 2005, he has been one of the directors of the "Hahn-Schickard-Institut für Mikro- und Informationstechnik" in Villingen-Schwenningen and Freiburg, Germany. In 2000, he spent half a year on a research project with the Sensor Division, Motorola, Phoenix, AZ, USA. During a research contract with Intel Inc., Santa Clara, CA, USA, in 2006, he worked on a high-resolution, wide-bandwidth accelerometer. A sabbatical leave at Columbia University, New York, NY, USA, in 2017, has led to creative and productive collaboration in the area of biomedical applications. His research interests are the design of low-voltage/low-power mixed-signal CMOS circuits, energy harvesting electronics, sensor readout circuits, as well as analog-to-digital converters. Additional research activities concentrate on motion and vibration energy transducers as well as on inertial sensors and sensor fusion.

Dr. Manoli is a member of VDE, Phi Beta Kappa, and the Mortar Board. He was one of the first five fellows nominated and selected for a fellowship at the Thomas Mann House in Pacific Palisades, CA, USA, in 2018. He and his group have received the best paper awards at the European Solid-State Circuits Conference (ESSCIRC) 1988, 2009, and 2012, PowerMEMS 2006, MWSCAS 2007, and MSE-2007. The MSE-2007 Award was granted for SpicyVOLTsim (www.imtek.de/svs), a web-based application for the animation and visualization of analog circuits for which he also received the Media Prize of the University of Freiburg in 2005. Further developments of SpicyVOLTsim were supported with a "Fellowship for Innovations in University Teaching" of the Baden-Wuerttemberg Foundation in 2011. He was the first to receive the Best Teaching Award of the Faculty of Engineering when it was introduced in 2008. For his creative contributions to interactive teaching of microelectronics, he has also received the Excellence in Teaching Award of the University of Freiburg and the Teaching Award of the State of Baden-Württemberg, both in 2010. He was the Program Chair in 2001 and the General Chair in 2002 of the IEEE International Conference on Computer Design (ICCD). He has served as a Distinguished Lecturer of the IEEE and on the Senior Editorial Board of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS and in addition as a Guest Editor for the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS. He is on the Editorial Board of the *Journal of Low Power Electronics*. He has served on the committees of a number of conferences, such as the International Solid-State Circuits Conference (ISSCC), ESSCIRC, the International Electron Devices Meeting (IEDM), and ICCD.