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Letter

Low-voltage organic transistors with steep subthreshold slope fabricated on commercially available paper

Ute Zschieschang *, Hagen Klauk

Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany

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ABSTRACT

Organic thin-film transistors were fabricated directly on the surface of commercially available cleanroom paper using the vacuum-deposited small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT). A thin, high-capacitance gate dielectric that allows the TFTs to be operated with low voltages of 2 V was employed. The TFTs have a charge-carrier mobility of 1.6 cm^2/Vs, an on/off current ratio of 10^6, and a subthreshold slope of 90 mV/decade. In addition, the TFTs also display a very large differential output resistance, which is an important requirement for applications in analog circuits and active-matrix displays.

Organic thin-film transistors (TFTs) create the possibility of implementing a wide range of electronic systems, such as sensors, information displays and integrated circuits, on a wide variety of substrates, including glass [1], textiles [2], plastics [3], and paper [4]. Paper is particularly intriguing, because unlike plastics, paper is a naturally renewable and easily recyclable material [4,5]. And while the performance of early organic TFTs fabricated on paper [6,7] used to be substantially inferior to that of organic TFTs fabricated on glass or plastics, there have recently been several encouraging reports on the successful realization of organic TFTs with impressive carrier mobilities and large on/off current ratios on a variety of types of paper.

For example, Li et al. [8] fabricated bottom-gate, top-contact organic TFTs on commercially available photo paper covered with a 3 μm thick parylene protection coating. They employed a 500 nm thick Cytop gate dielectric and the soluble small-molecule semiconductor 2,7-dioctyl[1]benzothieno[3,2-*b*][1]benzothiophene (C_8-BTBT), both of which were deposited by spin-coating. The TFTs were operated with gate-source voltages of 40 V and had a channel length of 50 μm, a carrier mobility of 1.3 cm^2/Vs, an on/off ratio of 10^8, and a subthreshold slope of 2 V/decade.

Rather than relying on commercially available paper, Fujisaki et al. produced smooth, transparent substrates from wood-based cellulose nanofibers [9]. The substrates were coated with a 2 μm thick planarization layer, and bottom-gate, bottom-contact TFTs were fabricated with a 300 nm thick polymer gate dielectric and the soluble small-molecule semiconductor Merck lisicon S1200. The source/drain contacts were patterned by photolithography and wet etching to define a channel length of 10 μm, which is the shortest channel length reported for organic TFTs on paper. The TFTs were operated with voltages of 20 V and had a carrier mobility of 1.3 cm^2/Vs, an on/off ratio of 10^8, and a subthreshold slope of 0.84 V/decade.

Minari et al. reported top-gate TFTs based on solution-printed Au nanoparticle source and drain contacts and solution-crystallized C_8-BTBT on commercially available, parylene-coated photo paper [10]. These TFTs had a channel length of 100 μm, an operating voltage of 40 V, an on/off ratio of 10^6, a subthreshold slope of 1.4 V/decade, and a carrier mobility of 2.5 cm^2/Vs, which is the largest mobility reported for organic TFTs on paper to date.

Peng et al. fabricated bottom-gate, top-contact TFTs directly on the surface of commercially available printing paper [11,12]. As the semiconductor, Peng et al. employed dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) [13–15], a vacuum-deposited small-molecule semiconductor that provides a unique combination of large carrier mobility and long-term air stability [15–17]. The gate electrodes and the source and drain contacts were defined using screen-printed Ag paste, and the gate dielectric was a layer of parylene with a thickness of 680 nm [11] or 2 μm [12]. The TFTs had channel lengths of 60 or 85 μm, and depending on the gate-dielectric thickness, they were operated with voltages of 30 or 80 V and had a carrier mobility of up to 0.56 cm^2/Vs, an on/off ratio of 10^7, a subthreshold slope of 0.9 V/decade, and a cutoff frequency of up to 50 kHz.

Bottom-gate, bottom-contact polymer TFTs with inkjet-printed gate electrodes and source/drain contacts, a 200 nm thick screen-printed polymer gate dielectric, and spin-coated poly(2,5-bis(3-tetradecyl-thiophen-2-yl)thieno[3,2-b]thiophene)

* Corresponding author.
E-mail address: U.Zschieschang@fkf.mpg.de (U. Zschieschang).

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(pBTTT) as the semiconductor fabricated on commercially available packaging paper covered with two planarization coatings were reported by Grau et al. [18]. These TFTs operated with voltages of 50 V and had a channel length of 25 μm, a carrier mobility of 0.086 cm^2/Vs, an on/off ratio of 10^4, and a subthreshold slope of 18 V/decade.

Most recently, Wang et al. [19] reported top-gate TFTs based on a phase-separating blend of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) and poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) and a 75 nm thick Cytop/Al_2O_3 double-layer gate dielectric with a capacitance of 31 nF/cm^2 fabricated on cellulose nanocrystal substrates covered with a 30 nm thick Al_2O_3 coating. The TFTs were operated with voltages of 10 V and had a channel length of 180 μm, a carrier mobility of 0.23 cm^2/Vs, an on/off ratio of 10^4 and a subthreshold slope of 0.9 V/decade. Similar to the TFTs reported by Peng et al. [11,12], and in contrast to the TFTs in references [8–10,18], the TFTs reported by Wang et al. showed the desirable enhancement-mode behavior, *i.e.*, the drain current of these TFTs was close to zero at zero gate-source voltage, so that integrated circuits based on these TFTs would require only one power supply.

Here we demonstrate bottom-gate, top-contact organic TFTs with enhancement-mode characteristics fabricated directly on the surface of commercially available paper, without applying a protective or planarization coating. A thin hybrid organic/inorganic gate dielectric with a large capacitance of 600 nF/cm^2 was employed, so that the TFTs can be operated with low voltages of about 2–3 V and have a subthreshold slope of 90 mV/decade, which is to our knowledge the steepest subthreshold slope reported to date for organic TFTs on paper. A steep subthreshold slope, ideally as close as possible to the room-temperature limit of 60 mV/decade, is highly beneficial, especially for applications in low-voltage, low-power integrated circuits for portable (*i.e.*, battery-powered) devices.

The paper on which the TFTs were fabricated is commercialized as cleanroom paper under the brand Galaxy® (Clear & Clean GmbH, Lübeck, Germany). It has a thickness of 115 μm and a specific weight of 100 g/m^2, and its surface is sealed with particle-binding polymers. The TFTs were fabricated in the bottom-gate, top-contact (inverted staggered) architecture. 40 nm thick aluminum was evaporated directly onto the surface of the paper through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the gate electrodes. The aluminum was briefly exposed to an oxygen plasma to create an aluminum oxide (AlO_x) layer with a thickness of about 3.6 nm, followed by immersing the substrate into a 2-propanol solution of *n*-tetradecylphosphonic acid (PCI Synthesis, Newburyport, MA, U.S.A.) to form a self-assembled monolayer (SAM) with a thickness of about 1.7 nm on the surface of the oxidized gates, resulting in an AlO_x/SAM gate dielectric with a thickness of about 5.3 nm [20,21]. A 30 nm thick layer of the high-mobility, air-stable small-molecule semiconductor DNTT [13–16,21–23] (Sigma Aldrich) was vacuum-deposited through a shadow mask, followed by the deposition of 30 nm thick gold through another shadow mask to define source/drain contacts with a channel length of 40 μm and a channel width of 200 μm. The maximum process temperature is 60 °C, which is the substrate temperature during the DNTT deposition. Except for the formation of the alkylphosphonic acid SAM that serves as part of the gate dielectric, this is an all-dry fabrication process that does not require any photoresists, solvents, developers or etchants, and if necessary, even the SAM can be formed by a dry process [24,25]. All electrical measurements were performed in ambient air at room temperature under weak yellow laboratory light. Fig. 1 shows the chemical structure of the semiconductor DNTT, a schematic cross-section of the TFTs, and a photograph of a TFT.

The unit-area capacitance and the leakage-current density of the AlO_x/SAM gate dielectric were measured on dedicated, shadow-mask-patterned Al/AlO_x/SAM/Au capacitors with an area of 4×10^{-4} cm^2 that were fabricated on paper along with the transistors. A total of 45 capacitors on three substrates were analyzed. The results are summarized in Fig. 2. For frequencies between 10 Hz and 100 kHz, the measured unit-area capacitance is about 600 nF/cm^2, with a standard deviation of 7%. The leakage-current density reaches a maximum of 1×10^{-6} A/cm^2 (average: 4×10^{-7} A/cm^2) at an applied voltage of −2 V (which is the biasing condition that resembles the situation of a negative gate bias in a transistor) and 2×10^{-5} A/cm^2 (average: 1×10^{-5} A/cm^2) at a voltage of +2 V. These values are similar to those previously measured on Al/AlO_x/SAM/Au capacitors fabricated on glass substrates [26], which indicates that the surface roughness of the substrate does not have a significant influence on the electrical properties of the AlO_x/SAM dielectric. The observation that the leakage-current density measured at positive voltages is larger by about one order of magnitude than the leakage-current density measured at negative voltages is possibly related to the work function difference between the Al bottom electrode and the Au top electrode, which likely results in different energy barriers at either side of the dielectric [27].

Typical electrical characteristics of the TFTs measured shortly after fabrication are summarized in Fig. 3. The output curves (Fig. 3a) indicate good linearity at small drain-source voltages and good saturation behavior for larger drain-source voltages. The small-signal (*i.e.*, differential) output resistance (*i.e.*, the inverse of the slope of the drain current *vs.* drain-source voltage curves in the saturation regime) ranges from 10^8 Ω at a gate-source voltage of −2.0 V to 10^{10} Ω at a gate-source voltage of −1.0 V (see Fig. 3b for a magnification of the output curves measured at these two gate-source voltages). These values are greater by at least two orders of magnitude than those of the TFTs reported in references [6–12,18,19]. A large differential output resistance is highly beneficial for applications in which the transistors are employed as current mirrors or current sources, for example in analog amplifiers [28–30] or to drive light-emitting diodes in active-matrix displays with a conventional (*i.e.*, continuous-excitation) pixel design [31,32].

The transfer characteristics (Fig. 3c) indicate the desirable enhancement-mode behavior (threshold voltage of −0.8 V, independent of the drain-source voltage) and a subthreshold slope of 90 mV/decade (see also Fig. 3d), which is to our knowledge the steepest subthreshold slope reported to date for organic TFTs on paper. (For an electrolyte-gated metal-oxide TFT with a dual-gate structure fabricated on paper coated with a 2 μm thick SiO_2 planarization layer, a subthreshold slope of 80 mV/decade has recently been reported [33]. For organic TFTs on plastic substrates, subthreshold slopes as steep as 65 mV/decade have been reported [34,35].) The field-effect mobility extracted from the transfer characteristics in the saturation regime at a drain-source voltage of −2.0 V is about 1.6 cm^2/Vs (see Fig. 3e). This is the second-largest mobility reported for organic TFTs on paper, second only to the mobility of 2.5 cm^2/Vs reported by Minari et al. for solution-crystallized C_8-BTBT TFTs [10]. The on/off current ratio of our DNTT TFTs is 10^6, which is smaller by two orders of magnitude than the on/off ratios reported by Li et al. [8] and Fujisaki et al. [9]; however, their TFTs required significantly larger operating voltages. A literature summary of the electrical properties of organic TFTs fabricated on paper is provided in Table 1.

Fig. 4 shows how the carrier mobility of the TFTs evolves over time when the substrate is stored in ambient air with a humidity of about 50% under weak yellow laboratory light. Over a period of two months, the subthreshold slope remains below 100 mV/decade and the on/off ratio remains close to 10^6, while

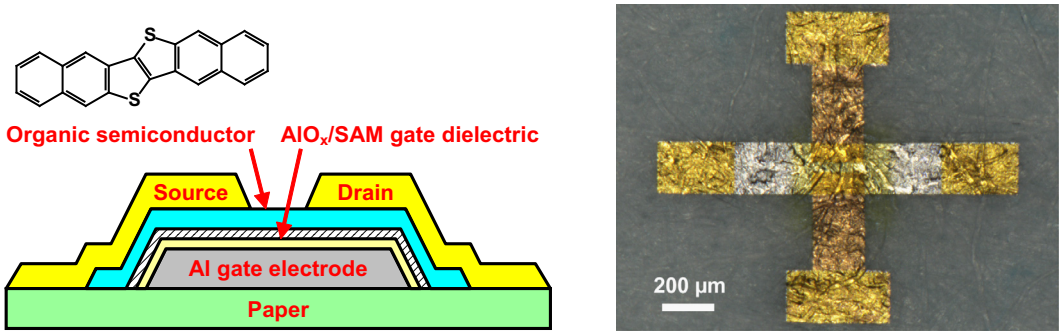

Fig. 1. Chemical structure of the organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT), schematic device cross-section, and photograph of a DNTT transistor with a channel length of 40 µm fabricated on paper.

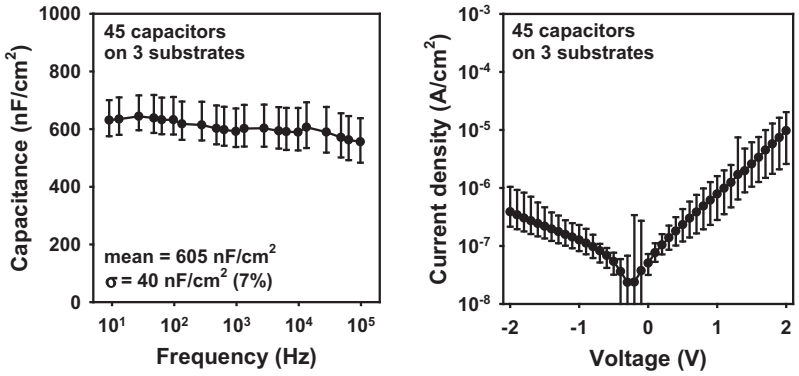

Fig. 2. Unit-area capacitance and leakage-current density of the AlO_x/SAM gate dielectric, measured on dedicated Al/AlO_x/SAM/Au capacitors with an area of 4×10^{-4} cm^2 fabricated on paper. For the leakage-current measurements, the electric potential was applied to the Al bottom electrode, with the Au top electrode held at ground potential. The error bars indicate the full range of values measured on 45 capacitors fabricated on three different substrates; the data points indicate the average values.

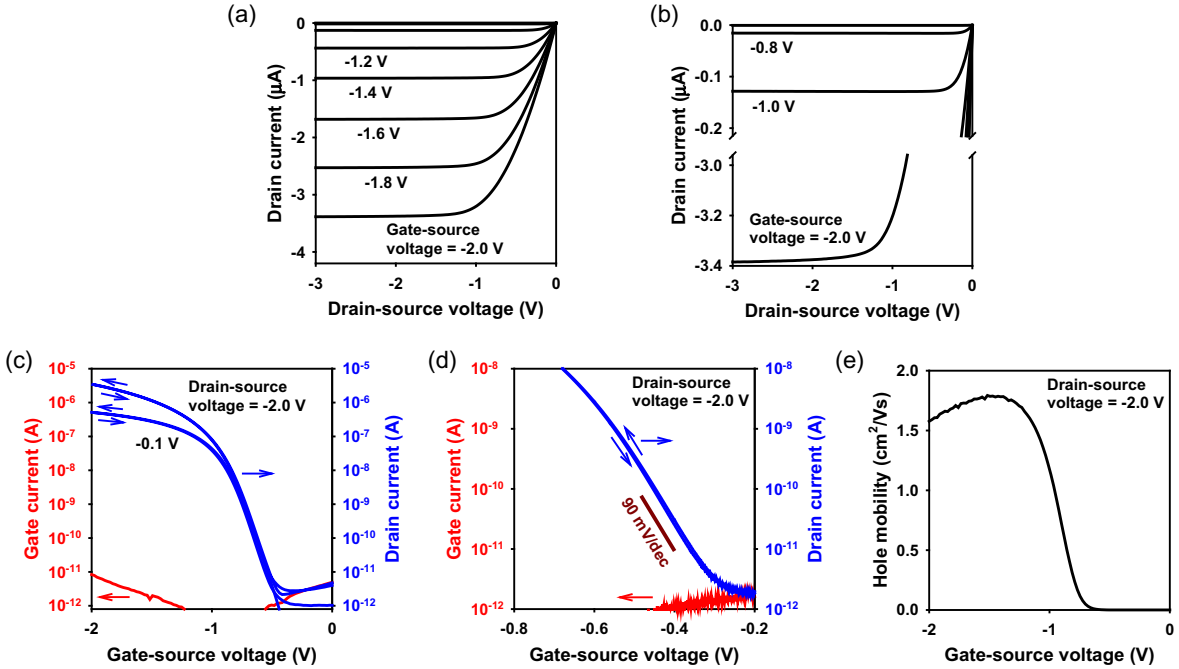

Fig. 3. Electrical characteristics of a DNTT TFT fabricated on paper. The transistor has a channel length of 40 µm and a channel width of 200 µm. (a) Output characteristics, showing good linear and saturation behavior. (b) Large differential output resistance in the saturation regime, highlighted for the output curves measured at gate-source voltages of −1 and −2 V. (c) Transfer characteristics for drain-source voltages of −0.1 and −2 V. (d) Subthreshold characteristics, indicating a slope of 90 mV/decade. (e) Field-effect mobility as a function of the applied gate-source voltage.

Table 1
Comparison of the properties of organic TFTs fabricated on paper reported in literature.

References	Planarization coating	Gate dielectric thickness	Gate dielectric capacitance (nF/cm^2)	Channel length (μm)	Gate-source voltage (V)	Carrier mobility (cm^2/Vs)	On/off ratio	Subthreshold slope
[6]	PVP	270 nm	12	50	30	0.2	10^5	1.8 V/dec
[7]	Parylene	250 nm	13	25	40	0.086	10^4	n/a
[8]	Parylene	500 nm	3.7	n/a	40	1.3	10^8	2.0 V/dec
[9]	Polymer	300 nm	12	10	20	1.3	10^8	0.84 V/dec
[10]	Parylene	120 nm	12	100	40	2.5	10^6	1.4 V/dec
[11]	None	680 nm	4.1	85	30	0.39	10^6	0.9 V/dec
[12]	None	2 μm	1.4	60	80	0.56	10^7	1.4 V/dec
[18]	Kaolin/PVP	197 nm	16	25	50	0.086	10^4	18 V/dec
[19]	Al_2O_3	75 nm	31	180	10	0.23	10^4	0.9 V/dec
[21]	None	5.3 nm	600	30	3	0.2	10^5	110 mV/dec
This work	None	5.3 nm	600	40	2	1.6	10^6	90 mV/dec

"n/a" means that these parameters are not available in the cited publication.

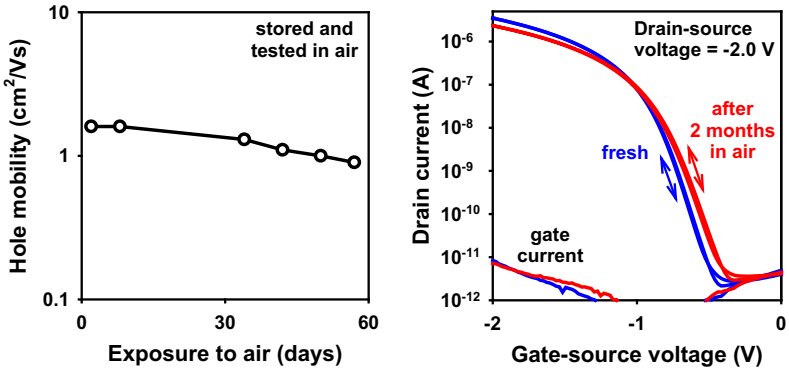

Fig. 4. Shelf-life stability of DNTT TFTs on paper.

the carrier mobility decreases by about 40%, from initially 1.6 cm^2/Vs to 0.9 cm^2/Vs. The chemical or physical mechanism(s) responsible for the observed mobility degradation remain unknown. Although an oxidation of the organic semiconductor cannot be entirely ruled out, it is somewhat unlikely, given the large oxidation potential of DNTT [13,15]. An alternative explanation is that the significant surface roughness of the paper substrate leads to a large surface area of the organic semiconductor layer, which in turn might render the semiconductor more vulnerable to the incorporation of ambient species into the grain boundaries of the organic thin-film, leading to a smaller inter-grain mobility [36].

In summary, we have fabricated organic transistors directly on the surface of commercially available paper, without applying a protective or planarization coating. Using the vacuum-deposited small-molecule organic semiconductor DNTT, we have achieved a carrier mobility of 1.6 cm^2/Vs, an on/off current ratio of 10^6, and a subthreshold slope of 90 mV/decade. In addition, the TFTs display a very large differential output resistance.

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