Macromodel for AC and Transient Simulations of Organic Thin-Film Transistor Circuits Including Nonquasistatic Effects

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***Abstract*— A charge-based macromodel for small-signal ac and transient analyses of organic thin-film transistors (TFTs) is presented. Due to the comparatively small charge-carrier mobility in organic TFTs, the dynamic behavior of the gate-field-induced carrier channel is greatly affected by the frequency of the applied gate–source and drain–source voltages. The model presented here is, therefore, based on the transmission-line model and shown to reproduce the results of frequency-dependent admittance measurements and numerical simulations of the transient switching behavior of organic TFTs fabricated in the staggered architecture with good accuracy. The model has been implemented in the hardware description language Verilog-A.**

***Index Terms*— AC analysis, capacitance model, charge-based model, macromodeling, nonquasistatic behavior, organic thin-film transistors (TFTs), transient analysis.**

I. Introduction

ORGANIC thin-film transistors (TFTs) are of interest for flexible, large-area electronics applications, such as active-matrix displays and integrated circuits [1]–[4]. The design of such systems requires simulations that ideally make use of compact models that describe the physical behavior of the devices in an accurate yet computationally efficient manner [5], [6]. In this article, we focus on the dynamic and nonquasistatic behavior of organic TFTs, which we describe using a macromodel based on a compact model. The reason why field-effect transistors show nonquasistatic behavior is that the charges have to flow through the transistor channel, which is characterized by an ohmic resistance. This resistance can be modeled by describing the transistor as a distributed *RC* transmission line, as reported previously for single-crystalline silicon MOSFETs [7] and polycrystalline silicon TFTs [8]. An approach to calculate the nonquasistatic capacitances of organic TFTs based on the transmission-line model reported in [8] was recently presented in [9]. This model also includes contact effects. In the modeling language Verilog-A, which is the industry standard for the implementation of compact models in circuit-design tools, it is not possible to access the frequency of applied ac signals. In [9], this problem was circumvented by passing the frequency of the applied ac signals as an additional, fixed parameter to the Verilog model. However, this workaround is suitable only for small-signal analyses involving only signals that are perfectly sinusoidal and of known frequency. Transient analyses, as described in [10], necessarily involve arbitrary signals being applied to the transistor terminals, making it impossible to pass the frequency as a fixed parameter to the model. A compact model for the transient behavior of electrolyte-gated organic transistors was presented in [11]. However, this model does not consider the charging of channel-capacitance elements through adjacent channel elements and is, thus, not able to fully capture nonquasistatic operation. The large-signal nonquasistatic behavior of organic TFTs has been modeled in [12] and [13] based on the current continuity equation discretized by a spline collocation. This model does not require the applied frequency as a parameter and is suitable for transient analyses, albeit at the cost of comparatively high complexity of the resulting equations and the Verilog-A model. In this article, we introduce a macromodel that also does not require the frequency of the applied signals as an additional parameter and is applicable to dc, small-signal ac, and transient analyses. In addition, this model is simple yet precise and easy to implement in Verilog-A without the necessity of solving the current continuity equation.

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II. Modeling Approach

The transistor is modeled as a distributed *RC* transmission line, which, for simplification purposes, consists of a finite

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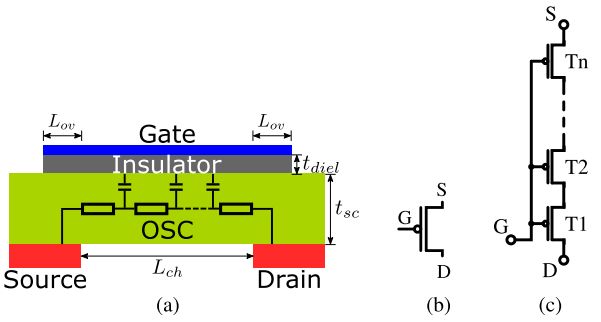

Fig. 1. (a) Schematic cross section of an organic TFT in the staggered architecture, including the transmission-line model. The capacitors represent the intrinsic channel capacitances, while the resistors represent sections of the ohmic channel resistance. (b) Symbol of the transistor. (c) Circuit schematic of that transistor modeled as a series connection of n transmission-line segments. The sum of the channel lengths of the n transmission-line segments in (c) is equal to the channel length of the transistor in (b).

number of (n) elements. Fig. 1(a) shows the schematic cross section of an organic TFT in the staggered architecture, including the transmission-line model. Each of the n capacitors in the transmission-line model represents a section of the intrinsic channel capacitance, and each of the n resistors is equivalent to a segment of the intrinsic channel resistance. The model specifically considers p-channel TFTs and does not take into account contact effects. Fig. 1(b) and (c) shows the symbol of the transistor and the circuit schematic of that transistor when modeled as a series connection of n transmission-line segments. In the transmission-line model, each of the n segments has a channel length of $L_{\mathrm{ch,single}}/n$, where $L_{\mathrm{ch,single}}$ is the channel length of the transistor in the model [14]. In terms of the dc behavior, the current that flows through the transmission line is identical to the drain current of the transistor in the model. However, its ac and transient behavior are more accurately captured by the transmission-line model, which correctly takes into account the charging and discharging of the channel capacitance of each segment through the channel resistance of the adjacent segments. The frequency dependence of the capacitances is, thus, implicitly accounted for [7], [14], [15].

In [16], a quasistatic dc compact model was developed, which was extended by a quasistatic charge model in [17]. These models have already been implemented in Verilog-A. In this work, the Verilog-A implementation of the quasistatic ac/dc model is extended by including the transmission-line model. The model implementation must also consider the influence of the parasitic gate-to-source and gate-to-drain overlap capacitances that specifically affect the properties of the outermost transistors T1 and Tn.

III. Model Verification

A. General Information

To verify the transmission-line model, staggered TFTs represented as transmission lines of various lengths were simulated in Cadence Virtuoso [18]. The reason for implementing the TFTs in the staggered, rather than the coplanar architecture, is that the influence of the parasitic gate-to-contact overlaps is more complex in staggered transistors than in coplanar transistors. AC and transient analyses were performed. In the following sections, the results of the ac analysis are compared with the experimental results reported in [15] and the results from TCAD Sentaurus [19] simulations. The results of the transient analysis are compared only to the simulation results. Table I summarizes the most important measured and simulated transistor parameters, including some of the values extracted for the dc compact model. These are the channel length L_{ch}, the channel width W_{ch}, the gate-to-contact overlap length L_{ov}, the fringing width w_{ovl}, the gate-dielectric thickness t_{diel}, the semiconductor thickness t_{sc}, the permittivity of the gate dielectric $\varepsilon_{\mathrm{diel}}$ and the permittivity of the semiconductor in full depletion $\varepsilon_{\mathrm{sc}}$, the low-field charge-carrier mobility κ, the power-law mobility factor β, the fringing fitting parameter δ_{fit}, the threshold voltage V_{T0}, and the subthreshold swing S [16], [20]. Table I contains both geometrical data and fitting parameters of the model, and the latter were determined from the dc analysis conducted prior to the ac and transient analyses.

TABLE I
Measured and Simulated Transistor Parameters

	Experimental [15]	TCAD AC	TCAD transient
L_{ch} [µm]	200	200	120
W_{ch} [µm]	400	1	1
L_{ov} [µm]	10	10	10
w_{ovl} [µm]	30	0	0
t_{diel} [nm]	5.3	5.3	5.3
t_{sc} [nm]	11	25	25
ε_{diel} [−]	3.37	3.9	3.9
ε_{sc} [−]	2.84	3	3
κ [$\mathrm{cm^2V^{\beta-1}s^{-1}}$]	2.05	0.9	0.9
β [−]	0.03	0.03	0.03
δ_{fit} [−]	0.5	1	1
V_{T0} [V]	-0.94	-0.79	-0.79
S [mV/dec]	70	90	90

B. AC Analysis

1) Experimental Data: In [15], an ac analysis of organic TFTs based on the vacuum-deposited small-molecule semiconductor dinaphto[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was presented. The ac analysis was performed by measuring the complex admittance $\underline{Y}$ using an LCR meter. As reported in [15] and [21], the prolonged continuous application of a gate–source voltage may cause a bias-stress-induced shift of the threshold voltage of the TFTs. We, therefore, treat the threshold voltage as a fitting parameter with a bias-stress-induced shift of about ± 0.5 V. During the ac measurements, the drain and source terminals of the TFT were shorted and connected to the low terminal of the LCR meter, and the gate electrode was connected to the high terminal. Based on the measured admittance $\underline{Y}$, the following calculations are performed: $C = \mathrm{Im}(\underline{Y}/\omega)$ and $G = \mathrm{Re}(\underline{Y}/\omega)$, where ω is the angular frequency. The capacitance C can be interpreted as the gate–gate capacitance C_{gg}. G is the loss of the transistor and can be interpreted as G_{gg}. When conducting an ac analysis in Cadence Virtuoso, the drain–source voltage is set to $V_{\mathrm{ds}} = -1$ mV because the Spectre solver implemented in Cadence

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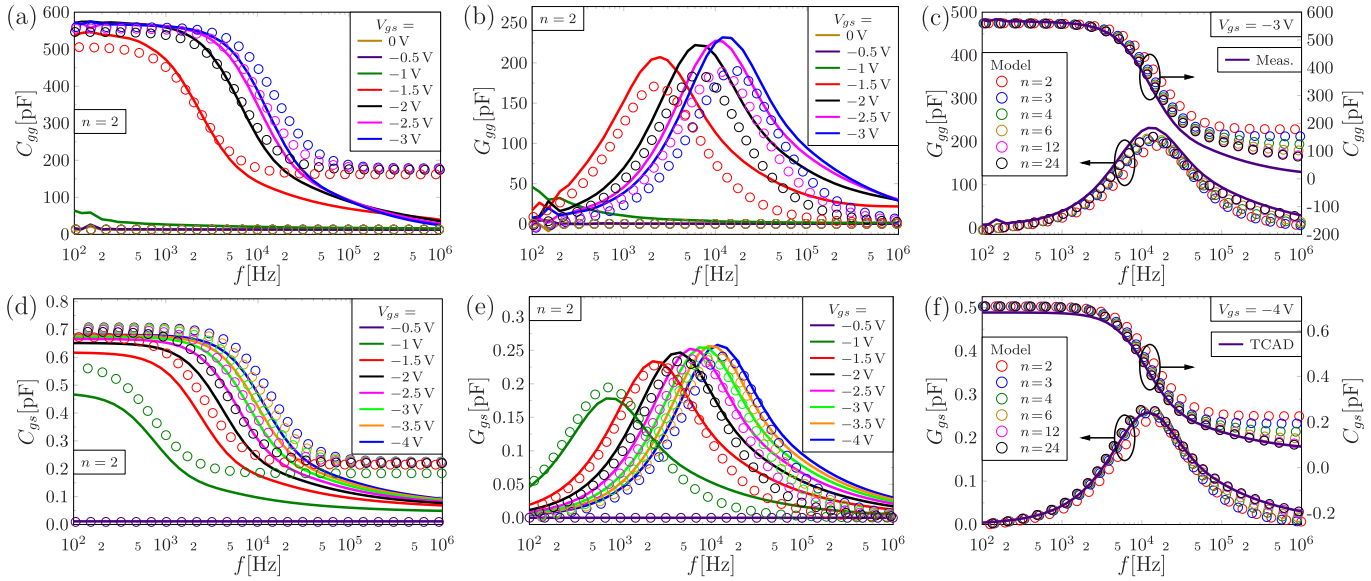

Fig. 2. (a) Gate–gate capacitance C_{gg} and (b) loss G_{gg} of an organic TFT for various gate–source voltages as a function of frequency. The TFT parameters are summarized in Table I. The experimental results reported in [15] are shown as lines, and the results of the transmission–line model are shown as symbols. In the model, the transmission line was partitioned into two segments (n=2). (c) C_{gg} and G_{gg} of the same TFT for a gate–source voltage of −3 V as a function of frequency. The experimental results are shown as lines, and the results of the transmission-line model are shown as symbols. In the model, the transmission line was partitioned into 2, 3, 4, 6, 12, or 24 segments. (d) Gate–source capacitance C_{gs} and (e) loss G_{gs} of a TFT for various gate–source voltages as a function of frequency. The results of the TCAD simulation are shown as lines, and the results of the transmission line model are shown as symbols. In the model, the transmission line was partitioned into two segments (n=2). (f) C_{gs} and G_{gs} of the same TFT for a gate–source voltage of −4 V as a function of frequency. The results of the TCAD simulation are shown as lines, and the results of the transmission-line model are shown as symbols. In the model, the transmission line was partitioned into 2, 3, 4, 6, 12, or 24 segments. The drain–source voltage V_{ds} is 0 V for the experimental data and −1 mV for the TCAD simulations and the model. For the simulator, the convergence conductance (g_{min}) was set to 1×10^{-13}S, which is several orders of magnitude smaller than the intrinsic channel conductances.

Virtuoso provides a better numerical stability when a nonzero voltage is applied to a series connection of elements. In the simulation, the complex admittance is determined as $\underline{Y} = I_{ds}/V_{gs}$. When the capacitance and the loss are calculated based on this definition, the result is C_{sg} and G_{sg}. However, as the drain–source voltage is close to zero, the transistor is always biased deep in the linear regime of operation so that $C_{sg} \approx C_{dg} \approx C_{gs} \approx C_{gd} \approx 1/2 \cdot C_{gg}$ and $G_{sg} \approx G_{dg} \approx G_{gs} \approx G_{gd} \approx 1/2 \cdot G_{gg}$.

In Fig. 2(a)–(c), the results of the ac analysis performed using the transmission-line model are compared with the experimental results reported in [15]. In Fig. 2(a) and (b), it can be seen that modeling the transistor as a transmission line consisting of only two segments already reproduces the measurement data to a certain degree. However, at high frequencies, the transmission-line model overestimates the capacitance and underestimates the conductance. Fig. 2(c) shows that the agreement between the results from the transmission-line model and the measurement data is notably improved by partitioning the transmission line into a larger number of segments.

2) TCAD Simulations: In this section, the results from the transmission-line model are compared with the results of the TCAD Sentaurus [19] simulation. In the simulation, the organic semiconductor is modeled as a crystalline semiconductor with a HOMO-LUMO energy gap of 3.38 eV (E_{LUMO} = 1.81 eV and E_{HOMO} = 5.19 eV). The electron mobility and the hole mobility were set to a constant value of 1 cm^{-2} V^{-1} s^{-1}. A Gaussian density-of-states (DOS) distribution with a maximum ($N_{t,DOS}$) of 1×10^{21} cm^{-3}, a standard deviation (σ_{DOS}) of 0.1 eV, and a shift ($E_V - E_{0,DOS}$) of 0.1 eV was assumed. As can be seen in Fig. 2(d)–(f), modeling the transistor as a transmission line consisting of only two segments already reproduces the simulation results to a certain degree. However, there are a few inaccuracies. For example, at a gate–source voltage of −1 V, there are deviations that are possibly related to the fact that the transition between the subthreshold and above-threshold regimes occurs at this gate–source voltage. Fig. 2(f) indicates that the agreement between model and simulation is improved by partitioning the transmission line into a larger number of segments. For example, partitioning the transmission line into 24 segments provides a perfect agreement between model and simulation for the gate–gate capacitance and the loss at a gate–source voltage of −4 V, but only a small improvement compared with 12 transmission-line segments. The desired accuracy can, thus, be achieved by tuning the number of transmission-line segments and observing the relative change in the resulting capacitances and losses. Deviations between the transmission-line model and the TCAD simulation results occur primarily at high frequencies so that, for frequencies up to about 20 kHz, partitioning the transmission line into four or six segments may already provide sufficient accuracy for this semiconductor.

C. Transient Analysis

In this section, the transmission-line model will be compared with the results of TCAD Sentaurus simulations by means of a transient analysis. In order to investigate the transient behavior of the organic TFTs, the drain–source voltage

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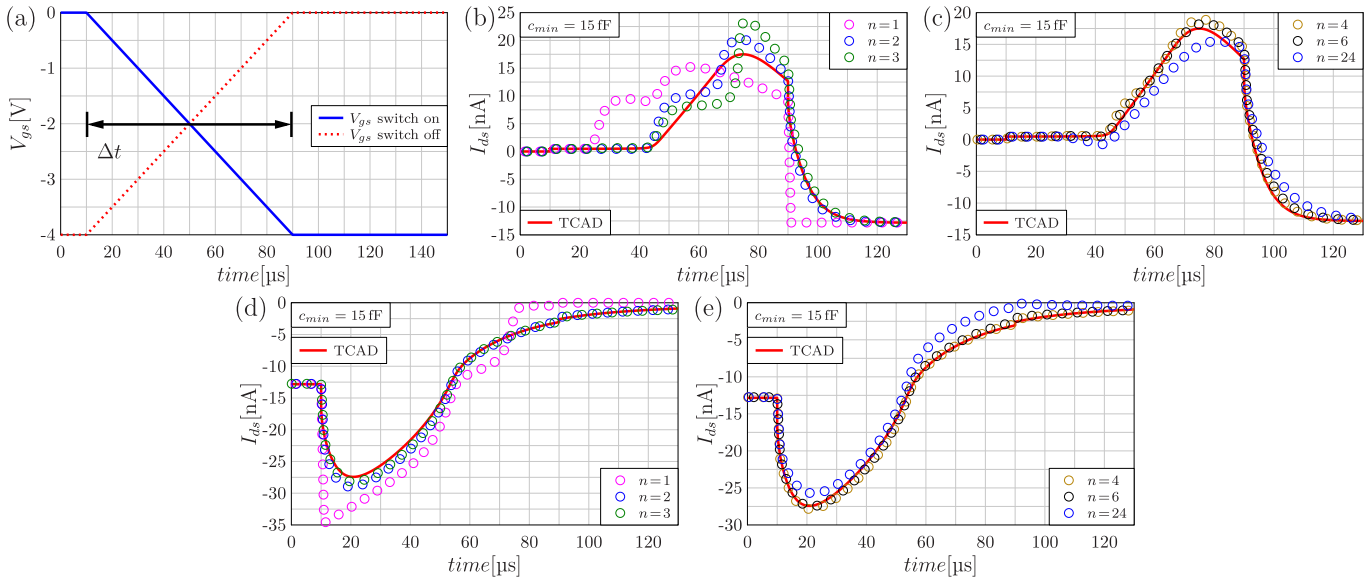

Fig. 3. (a) Gate–source-voltage transient defined for the TCAD simulations of the TFTs' switch-on (blue solid line) and switch-off behavior (dotted red line). After a waiting time of 10 μs, the gate–source voltage is ramped from 0 to -4 V or from -4 to 0 V, with a rise or fall time $\Delta t = 80$ μs. (b) and (c) Drain-current transient predicted by the transmission-line model (symbols) and the TCAD simulations (lines) in response to the switch-on process. (d) and (e) Drain-current transient predicted by the transmission-line model (symbols) and the TCAD simulations (lines) in response to the switch-off process. In the model, the transmission line was partitioned into 2, 3, 4, 6, or 24 segments. In the simulations with Cadence Virtuoso, a convergence capacitance (c_{min}) of 15 fF is implemented (see the Appendix). The drain–source voltage (V_{ds}) was set to -1 V.

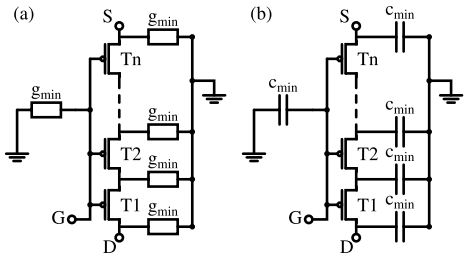

Fig. 4. Additional resistors (for dc and ac simulations) and capacitors (for transient simulations) automatically included by Cadence Virtuoso to improve convergence.

V_{ds} is set to a constant value, and the gate–source voltage V_{gs} is rapidly ramped up or down, as shown in Fig. 3(a). The duration of the ramp phase, Δt, greatly influences the drain-current response of the transistor. TFTs with a large channel length have larger capacitances and smaller channel conductance than short-channel TFTs, which leads to a significantly more pronounced charging effect in long-channel devices. We, therefore, perform the comparison between the results from the transmission-line model and those from the TCAD simulations on a long-channel TFT, having a channel length of 200 μm. The transmission line is partitioned into 2, 3, 4, 6, or 24 segments. As can be seen in Fig. 3(b)–(e), the transmission-line model is able to correctly reproduce the drain-current response obtained from the TCAD simulation. Both the model and the simulation produce a substantial overshoot or undershoot of the drain current in response to a rapid transient in the gate–source voltage, which is caused by the substantial charging (displacement) currents of the intrinsic and parasitic overlap capacitances. Once again, the accuracy of the model depends on the number of segments (n) into which the transmission line is partitioned: The quasistatic model ($n = 1$) leads to poor agreement with the TCAD simulation results. Partitioning the transmission line into two segments ($n = 2$) already notably improves the results. Increasing the number of segments beyond six yields diminishing returns. The reason is that for the simulations in Cadence Virtuoso, each circuit node must be connected to ground through a capacitor in order to achieve convergence (see the Appendix for further information).

IV. Conclusion

We have presented a macromodel to describe the nonquasistatic behavior of organic TFTs fabricated in the staggered device architecture. This model is based on a charge-based quasistatic compact model and has been extended by a numerical method to capture nonquasistatic effects. We have shown that by modeling the transistor as a transmission line partitioned into a number of RC segments, each of which is modeled as a transistor, it is possible to correctly reproduce the small-signal ac and transient characteristics of organic TFTs observed experimentally and in TCAD simulations. For an ac analysis, the agreement between the results from the model and those from measurements and simulations improve monotonically with increasing number of segments into which the transmission line is partitioned. For a transient analysis, the optimum number of segments required to achieve good agreement between the results from the model and those from TCAD simulations is approximately six for the simulation environment employed here due to the requirement of connecting each circuit node to ground through a capacitor in order to improve convergence. The model presented here correctly takes into account the frequency-dependent behavior in ac analyses and the nonquasistatic charging effects in transient

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analyses. The model is, thus, fully capable of providing accurate results in dc, small-signal ac, and transient circuit simulations.

Appendix: Convergence Issues

The model was executed in Cadence Virtuoso [18] using the Spectre solver. In order to achieve convergence while solving the system of nonlinear equations, the solver automatically connects each circuit node to ground through a resistor (for dc and ac simulations) or a capacitor (for transient simulations), as shown in Fig. 4. These modifications obviously lead to inaccuracies in the results, but especially the transient simulation will not converge without these additional capacitors. For the transient simulations, the capacitance of the convergence capacitors ($c_{\min}$) was set to 15 fF, which is substantially smaller than the gate–gate capacitance of the TFTs under investigation here when biased deep into the linear regime of operation ($C_{gg} \approx 900$ fF). Nevertheless, as $c_{\min}$ is not the sum but the per-node capacitance, the inaccuracy of the simulation results will increase with an increasing number of transmission-line segments.

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