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# Compact Modeling of Short-Channel Effects in Staggered Organic Thin-Film Transistors

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Abstract—This article introduces analytical compact models of short-channel effects in staggered organic thinfilm transistors (TFTs). The effects of subthreshold-swing degradation, threshold-voltage roll-off, and drain-induced barrier lowering (DIBL) on the static current-voltage characteristics of staggered TFTs are extracted from an analytical potential solution of the 2-D problem of the staggered geometry. This solution is derived by using the Schwarz-Christoffel transformation that leads to a complex mapping function linking the staggered geometry to an equivalent in another coordinate system for which an analytical potential solution exists. The technology CAD (TCAD) Software Sentaurus is used to verify the compact models. Finally, the closed-form and physics-based equations are incorporated into an existing compact current model and verified by measurements on staggered organic TFTs with channel lengths as small as 0.4  $\mu$ m fabricated on flexible plastic substrates by stencil lithography.

Index Terms—2-D potential solution, compact modeling, drain-induced barrier lowering (DIBL), organic thin-film transistors (TFTs), short-channel effects, threshold-voltage shift.

#### I. INTRODUCTION

MONG the current trends in the development of organic thin-film transistors (TFTs) [1] are the development of

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Fig. 1. (a) Schematic cross section and (b) simplified geometry of the staggered organic TFTs considered in this work [3], [7], where  $t_{diel}$  is the thickness of the gate dielectric,  $t_{sc}$  is the thickness of the semiconductor layer, and  $L_{ch}$  is the channel length for the TCAD simulations. (a) Real geometry. (b) Simplified geometry.

improved physics-based compact models to support efficient circuit design [2] and a more aggressive reduction of the channel length [3] to improve the dynamic performance of the TFTs [4]–[6] and circuits [7], [8]. However, decreasing the channel length of a field-effect transistor may introduce various short-channel effects, such as a nonlinearity of the output curves in the linear regime of operation (caused by the charge-injection barrier at the source contact [9]), a degradation of the subthreshold swing, and a dependence of the threshold voltage on the channel length (threshold-voltage roll-off) and the applied drain–source voltage drain-induced barrier lowering (DIBL) [10]. These short-channel effects arise from the field-induced modulation of the surface-potential barrier in the carrier channel of the transistor.

This article presents analytical, physics-based model equations for subthreshold-swing degradation, threshold-voltage roll-off, and DIBL that are suitable for implementation in organic-TFT compact models. The article is organized as follows: Section II presents an analytical potential solution of the Laplace equation for the staggered-geometry problem shown in Fig. 1. Since the short-channel effects are most pronounced in the subthreshold regime, i.e., in the absence of an accumulation channel, a solution of the Laplace equation is sufficient for compact modeling. This article extends the work presented in [11] by outlining the potential solution in greater detail and significantly improving the model in view of the physical interpretation. In Section III, models for subthreshold-swing degradation, threshold voltage roll-off, and DIBL are derived from the potential solution and verified using technology CAD (TCAD) simulations. Finally, all models are implemented into a current compact model initially presented in [12] and fitted to the current-voltage characteristics of organic TFTs obtained through TCAD simulations as well as to measured current-voltage characteristics of organic TFTs.

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Fig. 2. Simplification of the region of interest of the potential problem by redefining the boundaries shown as dotted red lines. (a) Closed-domain problem. (b) Simplified boundaries.



Fig. 3. Even- and odd-mode potential problems with the decomposition of the original boundary conditions. (a) Even mode. (b) Odd mode.

# II. ANALYTICAL CALCULATION OF THE SURFACE POTENTIAL

# A. Simplification of the Potential Problem

In order to define a potential problem that can be solved analytically in closed form and which adequately reflects the actual device geometry [Fig. 2(a)], the structure in Fig. 2(b) is introduced. Here, the boundaries of the region of interest shown as dotted lines are extended to infinity, which leads to a substantially simpler problem to solve. The boundary conditions for the source, drain and gate contacts are defined as follows:

$$\Phi_s = V_s - V_{bi} \tag{1}$$

$$\Phi_d = V_d - V_{bi} \tag{2}$$

$$\Phi_{\sigma} = V_{\sigma} - V_{fh}.$$
(3)

The corresponding built-in voltage  $V_{bi}$  and flatband voltage  $V_{fb}$  are composed as follows:

$$V_{bi} = \Phi_{m,s/d} - \left(\chi_{\rm sc} + \frac{E_g}{2q}\right) \tag{4}$$

$$V_{fb} = \Phi_{m,g} - \left(\chi_{\rm sc} + \frac{E_g}{2q}\right) \tag{5}$$

where  $\Phi_{m,g}$  is the work function of the gate metal,  $\Phi_{m,s/d}$  is the work function of the source/drain metal,  $\chi_{sc}$  is the electron affinity of the semiconductor, q is the elementary charge, and  $E_g$  is the difference between the energy of the lowest unoccupied molecular orbital (LUMO) and the energy of the highest occupied molecular orbital (HOMO) of the semiconductor. The fact that the geometry is symmetric makes it possible to decompose the potential problem into two separate problems, namely the even-mode potential problem and the odd-mode potential problem, as illustrated in Fig. 3 [13]. The geometry is not affected by the decomposition, but the boundary conditions of the two modes differ from those in the original problem, although they depend on the original boundary conditions defined in (1)–(3). The superposition of both modes yields the actual potential problem,



Fig. 4. Area of interest for both modes in the *z*-plane and the corresponding geometry in the *w*-plane in which a specific potential solution exists. (a) *z*-plane. (b) *w*-plane.

as illustrated in Fig. 2(b). An important aspect of the two modes is that their boundary conditions are defined along their axis of symmetry, as shown in Fig. 3. For the even-mode potential problem, these are Neumann boundaries (normal vector of the electric field  $\vec{E}_n = 0$ ), and for the odd-mode problem, these are Dirichlet boundaries ( $\Phi = 0$ ). Finally, the potential problem can be reduced to one half of the transistor, as illustrated by the hatched area in Fig. 3, and this substantially simpler geometry is sufficient to calculate the complete area of interest shown in Fig. 2(b). In order to derive a potential solution for the area of interest, the Schwarz-Christoffel transformation will be applied to obtain a complex conformal mapping function z = f(w). This will be discussed in Section II-B. This conformal mapping function z = f(w)will then be used in combination with an existing potential solution of a similar geometry that leads to a solution of the potential problem in Fig. 2. This will be the topic of Section II-C.

# B. Conformal Mapping Function

The Schwarz-Christoffel transformation is a conformal mapping technique that can be applied to derive a potential solution of the Laplace or Poisson equation, as these equations are invariant to this transformation [14]. The Schwarz-Christoffel transformation maps the boundaries of an arbitrary complex polygon defined in the plane z = x + zjy [Fig. 4(a)] by means of a complex conformal function (mapping function) onto the horizontal axis of the coordinate system in the plane w = u + jv [Fig. 4(b)]. Through this transformation, the area enclosed by the polygon [hatched area in Fig. 4(a)] is mapped onto the area located above the *u*-axis in the w-plane [hatched area in Fig. 4(b)]. The complexity of the mathematical expression of the mapping function depends on the number of vertices and on the relative change in the angle  $\gamma_{\alpha}\pi$  at each vertex. For the area of interest defined in Fig. 4(a), the important vertices and the relative changes in angle are summarized in Table I. Point 1 has no influence on the derivation of the mapping function, as it is located at an infinite distance from the origin in the *w*-plane. Each vertex  $z_{\alpha}$  in the z-plane is mapped onto its respective point  $w_{\alpha}$  in the w-plane. If the permittivity of the semiconductor ( $\epsilon_{sc}$ ) is different from that of the gate dielectric ( $\epsilon_{diel}$ ), a homogeneous domain, as described in [15], can be obtained by adjusting the thickness of the gate dielectric  $(t_{diel})$ 

$$\tilde{t}_{\rm diel} = t_{\rm diel} \epsilon_{\rm sc} / \epsilon_{\rm diel}.$$
 (6)

TABLE I MAPPING TABLE FOR ALL POLYGON VERTICES

	P2	P3	P4
$z_{lpha}$	0	$\infty j,$	$-\frac{Lch}{2} + (\tilde{t}_{diel} + t_{sc})j$
		$-\frac{Lch}{2}+\infty j$	2
$\gamma_{\alpha}\pi$	$\pi/2$	- π	$-\pi/2$
$\gamma_{lpha}$	1/2	1	-1/2
$w_{lpha}$	-1	1	p

Applying the values from Table I to the Schwarz– Christoffel transformation [14] leads to the following solution for the derivative of the mapping function according to Fig. 4:

$$\frac{dz}{dw} = C \prod_{(a)} (w - w_a)^{-\gamma_a} = C \frac{\sqrt{w - p}}{\sqrt{w + 1}(w - 1)}$$
(7)

where C is the scaling coefficient and p is the location of point 4 in the w-plane. To obtain a specific mapping function z = f(w) of the polygon in Fig. 4(a), (7) is integrated over w

$$z = f(w) = 2 C \ln(\sqrt{w - p} + \sqrt{w + 1}) - C\sqrt{2 - 2p} \cdot \tanh^{-1}\left(\frac{\sqrt{1 - p}\sqrt{w + 1}}{\sqrt{2}\sqrt{w - p}}\right) + D. \quad (8)$$

To determine the coefficient D, (8) is solved for point 2 ( $z_2 = f(-1) = 0$ ), which yields

$$D = -2C \ln(\sqrt{-1-p}).$$
 (9)

The points 1 and 3 in the *z*-plane are at an infinite distance from the origin of the coordinate system, which means that the lines to each point are parallel to each other. The distance between these parallel lines can be used to calculate the coefficients C and p. The former is determined by point 1 as follows [14]:

$$z_1'' - z_1' = j\pi C \text{ leads to } C = -\frac{\tilde{t}_{\text{diel}} + t_{\text{sc}}}{\pi}$$
(10)

where  $t_{sc}$  is the thickness of the semiconductor layer. The distance between  $z''_3$  and  $z'_3$  can be calculated using the values from Table I according to [14]

$$z_3'' - z_3' = -j\pi C (w_3 - w_2)^{-\gamma_2} (w_3 - w_4)^{-\gamma_4} -L_{\rm ch}/2 = -j\pi C (1+1)^{-1/2} (1-p)^{1/2}$$
(11)

where  $L_{ch}$  is the channel length. This equation can be solved for parameter p, which yields

$$p = 1 + \frac{L_{\rm ch}^2}{2\pi^2 C^2} = 1 + \left(\frac{L_{\rm ch}\epsilon_{\rm diel}}{\sqrt{2}(t_{\rm diel}\epsilon_{\rm sc} + t_{\rm sc}\epsilon_{\rm diel})}\right)^2.$$
 (12)

With this, all coefficients of the mapping function (8) have been solved. To solve the potential problem of the even-mode and the odd-mode potential problems illustrated in Fig. 3, an existing potential solution will be adapted and used in combination with the mapping function (8); this will be described in the following section.



Fig. 5. Geometry of two electrodes separated by a gap.

#### C. Adapting Potential Solution

Since the boundary conditions of the axis of symmetry in the even-mode and the odd-mode potential problems (Fig. 3) are different, the potential solutions must also differ, at least slightly. In order to obtain these potential solutions, the known potential solution of a geometry of two electrodes separated by a gap, as illustrated in Fig. 5, is adapted to the respective boundary conditions of each mode. For this geometry, the complex potential solution is given in [14] as follows:

$$P = \Phi + j\Xi = -\frac{j}{\pi}(\Phi_2 - \Phi_1)\cosh^{-1}\left(\frac{w}{a}\right) + \Phi_1. \quad (13)$$

The electrodes 1 and 2 in Fig. 5 correspond to the source-drain contacts and the gate electrode in Fig. 4(b), respectively. In both modes, the origin of the coordinate system has to be shifted to the location halfway between the two electrodes in the *w*-plane. Electrode 1 (source/drain) is located in Fig. 4(b) between points 1' ( $u = \infty$ ) and 4 (u = p) and remains the same for both modes. Electrode 2, however, is different in both modes.

For the even-mode potential problem, electrode 2 consists of the gate electrode between points 1"  $(u = -\infty)$  and 2 (u = -1). Thus, the origin of the coordinate system in Fig. 5 and (13) must be shifted to the location halfway between points 2 (u = -1) and 4 (u = p). This is accomplished by adding a term to the variable w in (13). In addition, the value of the parameter a must be adapted to the distance between points 2 and 4. The resulting new expression for  $a_e$  and the additional term  $w_e$  for the even-mode problem are

$$w_e = \frac{p-1}{2}, \quad a_e = \frac{p+1}{2}.$$
 (14)

For the odd-mode potential problem, the boundary conditions of the gate electrode and the axis of symmetry are identical, so they can both be treated as one electrode with a potential  $\Phi_{g,o} = 0 V$ . The respective electrode is located between points 1"  $(u = -\infty)$  and 3 (u = 1), which yields the following expressions for  $a_o$  and  $w_o$ :

1

$$w_o = 1 + \frac{p-1}{2}, \quad a_o = \frac{p-1}{2}.$$
 (15)

The modification of the potential solution in (13) combined with the mapping function derived in Section II-B provides potential solutions for the even-mode and the odd-mode problems in Fig. 3

$$P_{e/o} = -\frac{j}{\pi} (\Phi_{g,e/o} - \Phi_{s,e/o}) \cosh^{-1} \left( \frac{w - w_{e/o}}{a_{e/o}} \right) + \Phi_{s,e/o}.$$
(16)

Similarly, the potential in the right half can be obtained by adapting the boundary conditions and mirroring the solution.

Superposition by  $P = P_e + P_o$  yields the solution for the region of interest in Fig. 1(b). From this potential solution, an analytical expression for the surface potential will be derived in the following section.

# D. Surface Potential

The direct calculation of the surface potential at a particular point  $P_0(x_0, y_0)$  in the z-plane would require the inverse mapping function (8), which cannot be solved in closed form for  $w = f^{-1}(z)$ . However, it is possible to approximate the surface potential at the interface between the gate dielectric and the semiconductor layer. For this, the potential drop across the gate dielectric is assumed to be linear, which is a reasonable assumption as long as the gate-dielectric thickness is small compared to the other device dimensions. Consequently, the perpendicular electric field at the gate electrode can be used to calculate the voltage drop across the gate dielectric. Together with the known boundary condition at the gate electrode, the surface potential can thus be calculated as follows.

First, (16) is differentiated to obtain expressions for the electric field in the *w*-plane for both modes. Subsequently, both expressions are multiplied by the factor |dw/dz| to transform the electric-field solution from the *w*-plane onto the *z*-plane, as described in [11]

$$E_{z,e}(w) = \left| \frac{dw}{dz} \right| \frac{\Phi_{g,e} - \Phi_{s,e}}{\pi \sqrt{w + 1}\sqrt{w - p}}$$
(17)

$$E_{z,o}(w) = \left|\frac{dw}{dz}\right| \frac{\Phi_{g,o} - \Phi_{s,o}}{\pi\sqrt{w-1}\sqrt{w-p}}.$$
(18)

Determining the electric field along the gate electrode is relatively simple: Since all boundaries in the *w*-plane in Fig. 4 are located on the *u*-axis, the imaginary part *v* is zero, which leads to w = u. Finally, the surface potential can be calculated with the help of the boundary condition for the gate electrode as follows [11]:

$$\Phi_{\text{surf}}(u) = \Phi_g - (E_{z,e}(u) + E_{z,o}(u)) d_{\text{poi}}.$$
 (19)

The fitting parameter  $d_{\text{poi}}$  defines the distance between the point of interest and the gate electrode. For the surface potential at the interface between the gate dielectric and the semiconductor layer, the fitting parameter  $d_{\text{poi}}$  is set to  $d_{\text{poi}} = \tilde{t}_{\text{diel}}$ . The right half of the device can be calculated by replacing  $\Phi_{s,e}$  and  $\Phi_{s,o}$  in (17) and (18) with the respective boundary conditions  $\Phi_{d,e}$  and  $\Phi_{d,o}$  from Fig. 3.

# E. Channel Location

In staggered TFTs, the path taken by the electric current from source to drain depends on the gate potential. Fig. 6 shows results from TCAD simulations of the charge-density distribution along a vertical cutline at the center of the carrier channel, equidistant from source and drain (axis of symmetry in Fig. 3). The depth defines the distance between the point of interest and the gate electrode. When the transistor is operated above the threshold voltage, the channel is located close to the semiconductor-dielectric interface, as expected [16].



Fig. 6. Charge density along a vertical cutline located in the center of the carrier channel of a TFT operated above the threshold voltage (black line;  $V_{gs} = -1.5$  V) and operated below the threshold voltage (red line;  $V_{gs} = -0.1$  V).

However, when the transistor is operated below the threshold voltage, the charge flow from source to drain occurs far away from the semiconductor-dielectric interface, essentially in the plane that connects the semiconductor-source interface and the semiconductor-drain interface. This implies that the ability of the compact model to correctly capture the subthreshold swing and the DIBL requires knowledge of the surface potential at the point located halfway between the gate electrode and the source-drain contacts. To calculate this surface potential, the fitting parameter  $d_{poi}$  in (19) is set to  $d_{poi} = \tilde{t}_{diel} + t_{sc}$ by assuming that the potential profile in the vertical direction through the entire thickness of the gate dielectric and the semiconductor layer is linear. Although this approximation produces an error that increases with increasing  $d_{poi}$ , the results presented in Section III will show that the short-channel effects can nonetheless be modeled quite accurately.

#### **III. MODEL DEFINITION AND VERIFICATION**

In this section, the surface potential calculated in Section II will be applied to extract the potential-barrier lowering and derive expressions for the subthreshold-swing degradation, threshold-voltage roll-off and DIBL. The models thus derived will be verified by TCAD simulations. We also attempted to compare threshold-voltage roll-off and DIBL predicted by the compact model to measurement data, but this proved to be difficult, since the dependence of the threshold voltage on the channel length (threshold-voltage roll-off) and the applied drain-source voltage (DIBL) is smaller than its dependence on the density of charges trapped and released in the organic semiconductor and at the semiconductor-dielectric interface during and between measurements, so that the effects of threshold-voltage roll-off and DIBL are masked by the effects of dynamic charge trapping in the transistors [17]. Nevertheless, the models will be incorporated into a compact current model [12] and fit to the measured current-voltage characteristics of staggered organic TFTs with channel lengths between 0.4 and 1  $\mu$ m.

The TFTs were fabricated on flexible polyethylene naphthalate (PEN) substrates in the inverted staggered (bottomgate, top-contact) architecture by stencil lithography using high-resolution silicon stencil masks [3], [6], [7]. The gate dielectric is a combination of plasma-grown aluminum oxide and an alkylphosphonic acid self-assembled monolayer with a thickness of  $t_{diel} = 5.1$  nm, the semiconductor is a vacuum-deposited layer of dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT) with a nominal thickness of  $t_{sc} = 25$  nm, and the gold source and drain contacts have a thickness of  $t_{co} = 40$  nm [3], [7].

For the TCAD simulations, the TFT parameters were chosen as follows:  $t_{\text{diel}} = 5.1 \text{ nm}$ ,  $t_{\text{sc}} = 25 \text{ nm}$ ,  $t_{\text{co}} = 40$ ,  $\Phi_{m,g} = 4.1 \text{ V}$ ,  $\Phi_{m,s/d} = 5.19 \text{ V}$ ,  $\chi_{\text{sc}} = 1.81 \text{ V}$ ,  $E_{g,\text{sc}} = 3.38 \text{ eV}$ . For the organic semiconductor, a Gaussian density-of-states (DOS) model with the following parameters was assumed: density of states  $N_{\text{dos}} = 1 \times 10^{-21} \text{ cm}^{-3}$ , standard deviation  $\sigma = 0.1$  and a shift of the maximum position  $E_0 = 0.1 \text{ eV}$ . The charge-carrier mobility was assumed to be constant throughout the semiconductor. The potential-barrier height at the interface between the semiconductor and the source-drain contacts was set to  $\Phi_B = 0 \text{ V}$ .

# A. Subthreshold-Swing Degradation

The subthreshold swing of a long-channel transistor at room temperature (T = 300 K) can be written as

$$S = \alpha \frac{kT}{q} \ln(10) \approx 60 \frac{\text{mV}}{\text{dec}} \text{ with } \alpha = \frac{dV_g}{d\Phi_{\text{surf}}(u_{\text{mbh}})} = 1 \quad (20)$$

where k is the Boltzmann's constant, and T is the temperature.  $\Phi_{surf}(u_{mbh})$  is the maximum value of the surface potential at the position  $u_{mbh}$  in the w-plane. The parameter  $\alpha$  captures the derivative of the barrier height  $\Phi_{surf}(u_{mbh})$  with respect to the applied gate–source voltage  $V_{gs}$ . For organic TFTs with a channel length of less than about 1  $\mu$ m,  $\alpha > 1$ , which causes a degradation of the subthreshold swing. The short-channel parameter  $\alpha_{sc}$  can be determined from  $\Phi_{surf}$  as follows:

$$\alpha_{\rm sc} = \frac{dV_g}{\Phi_{\rm surf, u_{\rm mbh}}(V_{fb} + dV_g) - \Phi_{\rm surf, u_{\rm mbh}}(V_{fb})}.$$
 (21)

However, applying a drain-source voltage causes the maximum-barrier-height position  $u_{mbh}$  to shift from the center of the channel toward the source contact or the drain contact, depending on the polarity of the drain-source voltage. A physics-based analytical expression for the maximum-barrier-height position  $u_{mbh} = f(V_{ds}, L_{ch}, t_{diel}, t_{sc})$  cannot be derived in closed form. However, since the potential profile at the surface is relatively flat, it is sufficient to calculate the barrier height at the center of the channel independent of the drain-source voltage [11]. Equation (21) together with (19) and  $\Phi_{surf}(u = -1)$  leads to the following expression for the geometrically degraded subthreshold swing extracted at the center of the channel:

$$S_{\rm sc} = \frac{kT}{q} \ln(10)\alpha_{\rm sc} = \frac{kT}{q} \cdot \frac{\ln(10)}{1 - \frac{4(t_{\rm sc} + \tilde{t}_{\rm diel})d_{\rm poi}}{4(t_{\rm sc} + \tilde{t}_{\rm diel})^2 + L_{\rm ch}^2}}$$
(22)

where  $\tilde{t}_{die}$  is the stretched gate-dielectric thickness defined in (6). Fig. 7 shows the degradation of the subthreshold swing



Fig. 7. Degradation of the subthreshold swing upon reducing the channel length from 1 to 0.1  $\mu$ m calculated using (22) (green) and, for comparison, extracted from TCAD simulations of the surface potential in the channel (circles) and of the transfer characteristics (triangles). For a gate-dielectric thickness tdiel = 5.1 nm, the best agreement between the compact model and the TCAD simulations was obtained for  $d_{poi} = 29.1$  nm. Results for  $t_{diel} = 20$  nm are included to illustrate the scalability of the model regarding the gate-dielectric thickness.

upon reducing the channel length from 1 to 0.1  $\mu$ m calculated using (22) and, for comparison, extracted from TCAD simulations. For a gate-dielectric thickness  $t_{diel} = 5.1$  nm, the best agreement was obtained for  $d_{\text{poi}} = 29.1$  nm. The subthreshold swing was extracted from the TCAD simulations in two different ways, namely from the transfer characteristics and from the change in the surface potential in the channel, where according to Fig. 6 the current is expected to flow. This point of interest along the axis of symmetry is nearly equidistant from the gate electrode and the source–drain contacts. Fig. 7 shows that the results from the compact model [See (22)] are in good agreement with the results from the simulated surface potential in the channel, which confirms that the assumptions are reasonable. However, for channel lengths larger than about 0.3  $\mu$ m, they both deviate slightly from the results obtained from the simulated transfer characteristics. This deviation is attributed to the Gaussian DOS model which assumes a finite density of states in the bandgap of the organic semiconductor that is expected to degrade the subthreshold swing [12].

#### B. Threshold-Voltage Roll-Off

Among the parameters that control the height of the surface-potential barrier near the source and drain contacts and thus the threshold voltage of the transistor are the channel length  $L_{ch}$  and the applied drain-source voltage  $V_{ds}$ . All else (including  $V_{ds}$ ) being equal, decreasing the channel length will reduce the barrier height and thus the threshold voltage; this is referred to as threshold-voltage roll-off. For the following analysis, the threshold voltage will be extracted for  $V_s = V_d = 0$  V, so that regardless of the channel length, the maximum-barrier-height position  $u_{mbh}$  will be in the center of the channel, equidistant from source and drain, and thus (19) will be solved for  $u_{mbh} = -1$ . When the gate-source voltage is equal to the flatband voltage ( $V_g = V_{fb}$ ), i.e., in the absence of an accumulation channel, the potential problem is defined



Fig. 8. Threshold-voltage roll-off upon reducing the channel length from 1 to 0.1  $\mu$ m calculated using (23) (green line) and compared to TCAD simulations of the surface potential in the channel (black circles) and of the transfer characteristics (red triangles). For a gate-dielectric thickness  $t_{diel} = 5.1$  nm, the best agreement between the compact model [see (23)] and the TCAD simulations with  $t_{diel} = 5.1$  nm was obtained for  $d_{poi} = 5.1$  nm. Results for  $t_{diel} = 20$  nm are included to illustrate the scalability of the model regarding the gate-dielectric thickness.

by the Laplace equation. Since the surface potential in a long-channel transistor at the maximum-barrier-height position,  $\Phi_{\text{surf},long-channel}(u = -1)$ , is equal to zero, the resulting threshold-voltage roll-off can be written as

$$\Delta V_{T,\text{roll-off}} = -\Phi_{\text{surf,short-channel}}(-1)$$
  
=  $-V_{bi} \frac{4(t_{\text{sc}} + \tilde{t}_{\text{diel}})d_{\text{poi}}}{4(t_{\text{sc}} + \tilde{t}_{\text{diel}})^2 + L_{\text{ch}}^2}$  (23)

where  $\Phi_{\text{surf,short-channel}}$  is given by (19) for the case of the short-channel transistor having a channel length  $L_{ch}$ . Fig. 8 shows the threshold-voltage roll-off upon reducing the channel length from 1 to 0.1  $\mu$ m calculated using (23) and, for comparison, obtained from TCAD simulations of the transfer characteristics and the surface potential in the channel. For a gate-dielectric thickness  $t_{diel} = 5.1$  nm, the best agreement was obtained for  $d_{poi} = 5.1$  nm. For the extraction from the simulated transfer characteristics, the  $g_m/I_d$  method [18] was used. Despite general inconsistencies in the extraction of the threshold voltage of organic TFTs using different methods [19], Fig. 8 shows that the results from the compact model [See (23)] are in good agreement with the results from the TCAD simulations, both for the extraction from the simulated change in the surface potential in the channel and for the extraction from the simulated transfer characteristics.

#### C. Drain-Induced Barrier Lowering

When the drain-source voltage is increased, the height of the surface-potential barrier along the current path is decreased, causing a shift of the threshold voltage, defined here as  $\Delta V_{\text{DIBL}}$ . The decrease in potential-barrier height is accompanied by a shift of the maximum-barrier-height position  $u_{\text{mbh}}$  from the center of the channel toward the source contact. As shown previously [11], the effect of this shift of the maximum-barrier-height position on the accuracy of the model is quite small and will thus be ignored. To derive a closed-form



Fig. 9. DIBL-induced threshold-voltage shift  $\Delta V_{\text{DIBL}}$  for channel lengths from 1 to 0.1  $\mu$ m and  $V_{\text{ds}} = -1$  V calculated using (24) (green line) and, for comparison, obtained from TCAD simulations of the surface potential in the channel (black circles) and of the transfer characteristics (red triangles). For  $t_{\text{diel}} = 5.1$  nm, the best agreement between the compact model [see (24)] and the TCAD simulations was obtained for  $d_{\text{poi}} = 29.1$  nm. Results for  $t_{\text{diel}} = 20$  nm are included to illustrate the scalability of the model regarding the gate-dielectric thickness.

compact model, the maximum-barrier-height position will be assumed to be located in the center of the channel, yielding the following expression for the DIBL-induced threshold-voltage shift:

$$\Delta V_{\text{DIBL}} = \Phi_{\text{surf}}(V_{\text{ds}}) - \Phi_{\text{surf}}(V_{\text{ds}} = 0 \text{ V})$$
  
=  $V_{\text{ds}} \frac{2(t_{\text{sc}} + \tilde{t}_{\text{diel}})d_{\text{poi}}}{4(t_{\text{sc}} + \tilde{t}_{\text{diel}})^2 + L_{\text{ch}}^2}.$  (24)

Fig. 9 shows the DIBL-induced threshold-voltage shift  $\Delta V_{\text{DIBL}}$ for channel lengths from 1 to 0.1  $\mu$ m calculated using (24) and, for comparison, obtained from TCAD simulations of the transfer characteristics and the surface potential in the channel. For the extraction from the simulated transfer characteristics, the drain-source voltage was set to  $V_{ds1} = 0$  V and  $V_{ds2} = -1.5$  V. For a gate-dielectric thickness  $t_{diel} =$ 5.1 nm, the best agreement was obtained for  $d_{poi} = 29.1$  nm. The observation that the compact model slightly overestimates the DIBL-induced threshold-voltage shift  $\Delta V_{\text{DIBL}}$  is likely due to the fact that the shift of the maximum-barrier-height position  $u_{\rm mbh}$  from the center of the channel toward the source contact was ignored, as mentioned above. However, the excellent agreement between the results from the compact model [See (24)] and the results from the simulated transfer characteristics confirms the observation illustrated in Fig. 6 that in the subthreshold regime, most of the drain current flows not at the semiconductor-dielectric interface, but in the plane that connects the semiconductor-source interface with the semiconductor-drain interface. For accurate modeling of the DIBL, this must be taken into account.

### D. Implementation Into Current Model

The model equations for the subthreshold swing (22), threshold-voltage roll-off (23), and DIBL (24) have been implemented into the charge-based compact dc model published in [12]. In the following, we will apply the derived



Fig. 10. Transfer characteristics of staggered organic TFTs with channel lengths of 1  $\mu$ m, 0.5  $\mu$ m, and 0.4  $\mu$ m calculated using (27) (green lines) and, for comparison, obtained from measurements.

charge densities at the source end of the carrier channel  $(Q'_{\rm ms})$  and the drain end of the carrier channel  $(Q'_{\rm md})$ :

$$Q'_{\rm ms/d} = \frac{S_{\rm Traps}}{\ln(10)} \cdot C'_{\rm diel} \cdot LW \left\{ \exp\left(\frac{V_{\rm gs/d} - V_{\rm T0}}{S_{\rm Traps}/\ln(10)}\right) \right\}$$
(25)

where LW(*x*) is the first branch of the Lambert *W* function,  $C'_{\text{diel}}$  is the unit-area gate-dielectric capacitance, and  $V_{T0}$  is the long-channel-transistor threshold voltage. The subthreshold swing influenced by traps ( $S_{\text{Traps}}$ ) is defined as

$$S_{\text{Traps}} = \alpha_{\text{Traps}} \frac{kT}{q} \ln(10).$$
 (26)

The parameter  $\alpha_{\text{Traps}}$  captures the influence of traps in the organic-semiconductor layer and at the semiconductor-dielectric interface on the subthreshold swing. The equation for the drain current reflecting the drift-diffusion transport of quasi-free carriers in the semiconductor can be written in the well-known form [12]

$$I_{d} = \mu_{\rm eff} W_{\rm ch} \cdot \left(\frac{kT}{q} \cdot \frac{Q'_{\rm ms} - Q'_{\rm md}}{L_{\rm ch}} + \frac{Q'_{\rm ms}^2 - Q'_{\rm md}^2}{2L_{\rm ch}C'_{\rm ox}}\right) + \frac{V_{\rm ds}}{R_{\rm leak}}$$
(27)

where  $W_{ch}$  is the channel width,  $L_{ch}$  is the channel length,  $\mu_{eff}$  is the effective charge-carrier mobility of the organic semiconductor, and  $R_{leak}$  is a fitting parameter that accounts for a possible increase in the OFF-state drain current upon reducing the channel length. The effective charge-carrier mobility  $\mu_{eff}$ is derived using a power-law mobility model that captures the hopping transport typically observed in organic semiconductors and a contact-resistance model, as detailed in the Appendix. In order to implement the compact models for threshold-voltage roll-off [See (23)] and DIBL [See (24)], the threshold-voltage parameter  $V_{T0}$  for long-channel transistors is substituted by the following expression:

$$V_{T,sc} = V_{T0} - \Delta V_{T,roll-off} - \Delta V_{DIBL}.$$
 (28)

The subthreshold swing  $S_{\text{Traps}}$  in (25) is substituted with:

$$S_{\rm sc,traps} = \alpha_{\rm sc} \alpha_{\rm Traps} \frac{kT}{q} \ln(10).$$
 (29)

Both the influence of traps and the influence of the channel length on the subthreshold swing are thus taken into account by the compact current model.

TABLE II PARAMETER SETUP OF COMPACT MODEL

$L_{ch}$	$\mu_0$	β	$J_s$	$R_{sheet}$	$\alpha_{Traps}$	$R_{leak}$	$f_{hys}$
$[\mu m]$	$\left[\frac{cm^2V^\beta}{Vs^{-1}}\right]$	[]	$\left[\frac{A}{m^2}\right]$	$[\Omega]$	$\left[\frac{V}{V}\right]$	$[G\Omega]$	[]
$1.0 \\ 0.8 \\ 0.6 \\ 0.5 \\ 0.4$	$\begin{array}{c} 0.71 \\ 0.71 \\ 0.90 \\ 0.90 \\ 0.50 \end{array}$	0.52 0.52 0.85 0.93 1.05	1270 1270 750 750 490	2 2.5 6.5 10 9.5	2.713 2.990 4.199 4.367 4.871	3000 200 4 4 0.17	0.03 0.03 0.03 0.03 0.03 0.04

## E. Verification Using Measurements

In Section III-D, the model equations for the subthreshold swing, threshold-voltage roll-off, and DIBL were implemented into a compact current model. This model will be verified by fitting the results from the model to the measured transfer characteristics of staggered organic TFTs with channel lengths ranging from 1 to 0.4  $\mu$ m. To demonstrate the excellent scalability of the compact model, the fitting procedure was performed with the goal of maximizing the number of parameters whose values can be chosen independent of the channel length. Since the compact current model does not consider trapping-related hysteresis effects [17], the influence of these effects on the transfer characteristics of the transistors was accounted for by an empirical approach. We thus define a drain–source-voltage-dependent threshold-voltage shift due to trap filling as follows:

$$\Delta V_{\rm hys} = V_{\rm ds} \cdot f_{\rm hys} \tag{30}$$

where  $f_{\rm hys}$  is a fitting parameter determined by the sweep rate during the measurement of the transfer characteristics. Equation (30) assumes that the hysteresis manifests itself as a rigid shift of the transfer characteristics that can be described by a simple threshold-voltage shift. Finally,  $\Delta V_{\rm hys}$ was implemented into the compact current model in the same way as the DIBL model in Section III-D. The results are shown in Fig. 10. Table II summarizes those model parameters whose values vary from device to device. The fitting parameters  $\mu_0$  and  $\beta$  in (31) yield an effective charge-carrier mobility ( $\mu_{\rm eff}$ ) of approximately 1.5 cm<sup>2</sup>/Vs for gate–source voltages up to -3 V, as expected for staggered DNTT TFTs with AlO<sub>x</sub>/SAM gate dielectrics [3], [7], [20]. Table II indicates that with decreasing channel length, the reverse-biased saturation-current density of the Schottky barrier  $J_s$  decreases while the semiconductor sheet resistance  $R_{\text{sheet}}$  and the fitting parameter  $\alpha_{\text{Traps}}$  increase. The observation that  $R_{\text{sheet}}$  and  $\alpha_{\text{Traps}}$ show a dependence on the channel length may be surprising, given that all TFTs were fabricated on the same substrate using the same materials and the same process. One explanation is that the trap density is larger in the vicinity of the source and drain contacts than in the center of the channel, so that the effective trap density would increase with decreasing channel length. Also, a number of more or less realistic approximations had to made in the derivation of the compact models for the contact resistances [See (33) and (34)], which ultimately enter the equation for the effective charge-carrier mobility [See (32)]. The dependence of the fitting parameter  $R_{\text{leak}}$ on the channel length reflects the expected increase in the OFF-state drain current with decreasing channel length. The fitting parameter  $f_{hys}$  is independent of the channel length, since it is determined solely by the sweep rate during the measurement, which was identical during all measurements. The subthreshold-slope degradation, threshold-voltage roll-off and channel-length-dependent DIBL predicted by the model are in good agreement with the measurement data. For channel lengths below about 0.5  $\mu$ m, the leakage current dominates the subthreshold behavior, which the model is not able to capture.

#### **IV. CONCLUSION**

We have presented analytical and physics-based models of subthreshold-swing degradation, threshold-voltage rolloff and DIBL in staggered organic TFTs. The derivation of these models is based on a 2-D potential solution. The results from the models are in good agreement with results from TCAD simulations performed using Sentaurus. When the transistors are operated below the threshold voltage, the charge flow from source to drain occurs far away from the semiconductor-dielectric interface, essentially in the plane that connects the semiconductor-source interface and the semiconductor-drain interface. This must be taken into account in the calculation of the subthreshold swing and DIBL, since the surface potential at the maximum-barrier-height position along this path must be known for these calculations. For the calculation of the threshold-voltage roll-off, the transistors are assumed to be operating near the threshold voltage, with the carrier channel being located close to the semiconductor-dielectric interface.

Incorporating these models into a compact current model [12] significantly improves the accuracy of the model in predicting the current–voltage characteristics of short-channel TFTs. Parameters were extracted from the measured current–voltage characteristics of staggered organic TFTs with channel lengths between 0.4 and 1  $\mu$ m. The measurement data were fitted using similar model parameters, which confirms the scalability of the compact model with respect to the channel length.

#### APPENDIX

The power-law mobility model can be written as [12]

$$\mu = \mu_0 \cdot \left( Q'_{\rm ms} / C'_{\rm ox} \right)^{\rho} \tag{31}$$

where  $\mu_0$  is the low-field mobility factor and  $\beta$  is the power-law exponent. The effective carrier mobility  $\mu_{eff}$  is then determined by the field-independent (linear) contact resistance  $R_c$  and the field-dependent (nonlinear) resistance  $R_{sb}$  caused by the Schottky barrier at the source/channel interface [9], [12], [21]

$$\mu_{\rm eff} = \frac{\mu}{1 + \mu W_{\rm ch}(R_c + R_{\rm sb})Q'_{\rm ms}/L_{\rm ch}}.$$
 (32)

For the staggered transistor architecture considered in this article, the field-independent contact resistance  $R_c$  can be calculated according to [22] by taking into account the contact length  $L_c$  (essentially identical to the gate-to-contact overlap length) and an additional contribution of an extended contact length  $L_{\text{ext}}$ 

$$R_c = \frac{2R_{\text{sheet}}L_T}{W_{\text{ch}}} \coth\left(\frac{L_c + L_{\text{ext}}}{L_T}\right)$$
(33)

where  $L_T$  is the transfer length, defined as the contact length over which 63% of the charge exchange between contact and semiconductor occurs, and  $R_{\text{sheet}}$  is the sheet resistance of the semiconductor layer [22]. The field-dependent Schottkybarrier resistance  $R_{\text{sb}}$  can be calculated with the barrier height at the source/semiconductor interface  $\Phi_B$  [9]

$$R_{\rm sb} = \frac{V_{\rm gs} - V_{T0} - \frac{Q_{\rm ms}}{C_{\rm ox}'}}{J_s W_{\rm ch} l_{\rm inj} A^* T^2 \exp\left(-\frac{q(\Phi_B - \Delta\Phi_B)}{\eta kT}\right)}$$
(34)

where  $A^*$  is the Richardson constant,  $l_{inj}$  is the effective injection length,  $J_s$  is the reverse-biased saturation current, and  $\eta$  is a fitting parameter that accounts for the nonideality of the Schottky barrier. The Schottky barrier lowering  $\Delta \Phi_B$ in case of a staggered structure is as follows [9], [21]:

$$\Delta\phi_B = \sqrt{\frac{q(V_{\rm gs} - V_{T0} + \Phi_B - \frac{Q'_{\rm ms}}{C'_{\rm ox}})}{4\pi\epsilon_0\epsilon_r t_{\rm sc}}}.$$
 (35)

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