Charge-Based Model for the Drain-Current Variability in Organic Thin-Film Transistors Due to Carrier-Number and Correlated-Mobility Fluctuation

Aristeidis Nikolaou[®], Ghader Darbandy[®], Jakob Leise[®], Jakob Pruefer[®], James W. Borchert, Michael Geiger, Hagen Klauk[®], Benjamin Iñiguez, *Fellow, IEEE*, and Alexander Kloes[®], *Senior Member, IEEE*

Abstract—In this study, a consistent analytical chargebased model for the bias-dependent variability of the drain current of organic thin-film transistors is presented. The proposed model combines both charge-carrier-numberfluctuation effects and correlated-mobility-fluctuation effects to predict the drain-current variation and is verified using experimental data acquired from a statistical population of organic transistors with various channel dimensions, fabricated on flexible polymeric substrates in the coplanar or the staggered device architecture.

Index Terms— Carrier-number fluctuation, mobility fluctuation, organic thin-film transistors (TFTs), trap density, variability.

I. INTRODUCTION

I N ORGANIC thin-film transistors (TFTs), the semiconductor is usually a thin polycrystalline film of conjugated organic molecules [1]. Organic TFTs can often be fabricated at temperatures below 100 °C. This makes them promising for low-cost large-area flexible electronic circuits [2].

Drain-current variability can be perceived as the time-independent variation of the drain current of two or more nominally identical transistors under the same biasing conditions. Drain-current variability of organic-TFT-based circuits is commonly determined using circuit-based Monte

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Aristeidis Nikolaou, Jakob Leise, and Jakob Pruefer are with NanoP, TH Mittelhessen University of Applied Sciences, 35390 Giessen, Germany, and also with DEEEA, Universitat Rovira i Virgili, 43003 Tarragona, Spain (e-mail: aristeidis.nikolaou@ei.thm.de).

Ghader Darbandy and Alexander Kloes are with NanoP, TH Mittelhessen University of Applied Sciences, 35390 Giessen, Germany.

James W. Borchert, Michael Geiger, and Hagen Klauk are with the Max Planck Institute for Solid State Research, 70569 Stuttgart, Germany. Benjamin Iñiguez is with DEEEA, Universitat Rovira i Virgili, 43003 Tarragona, Spain.

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Fig. 1. Cross section of the organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) architecture.

Carlo simulations [3], mismatch modeling [4] or novel noise-based simulation approaches [5]. Here, a device-level charge-based variability model is introduced. The proposed physical model has two fitting parameters, can be applied directly to the experimental statistical population without the need for Monte Carlo simulations, and accurately describes the bias-dependent variability of organic TFTs, fabricated either in the coplanar or the staggered device architecture.

II. DEVICES AND MEASUREMENTS

Organic p-channel TFTs with channel lengths (L) of 2, 3, and 5 μ m and a channel-width-to-length ratio (W/L) of 10, were fabricated on a 125-µm-thick flexible polyethylene naphthalate (PEN) substrate in the inverted coplanar (bottom-gate, bottom-contact) device architecture (Fig. 1), using stencil lithography based on high-resolution silicon stencil masks [6]. The TFTs consist of 25-nm-thick aluminum gate electrodes, a 5.3-nm-thick hybrid AIO_x/SAM gate dielectric, 30-nm-thick gold (Au) source and drain contacts coated with a pentafluorobenzenethiol (PFBT) monolayer, and a 25-nm-thick vacuum-deposited layer of the small-molecule organic semiconductor 2,9-diphenyl-dinaphtho-[2,3-b:2',3'f]thieno[3,2-b]thiophene (DPh-DNTT) [7]. The maximum process temperature was 90 °C. For each channel length, 16 nominally identical TFTs were fabricated and characterized. The measurement protocol comprises transfer characteristics at a drain-source voltage (V_{DS}) of -3.0 V and gate-source voltages (V_{GS}) from 0 to -3.0 V with a step size of -50 mV, recorded at room temperature. In order to verify the proposed model for TFTs fabricated in the staggered device architecture, experimental data from [8], for bottom-gate top-contact DNTT TFTs with dimensions of $W/L = 10 \ \mu m/1 \ \mu m$, are used.



Fig. 2. (a) Transistor channel divided into a noisy element between positions *x* and $x + \delta x$ and two noiseless transistors of channel lengths *x* and *L* – *x*, respectively. (b) Small-signal representation.

III. DRAIN-CURRENT-VARIABILITY-MODEL DERIVATION

In this section, the impact of local charge-density fluctuations in the carrier channel as a source of the drain-current variability in nominally identical organic TFTs will be discussed. For the derived variability model, the charge-based organic-TFT model described in [9] will be used as the basis. The proposed current–voltage model provides a single current equation that is valid for all operation regions that can be obtained from

$$I_{\rm DS} = \mu W \left(\frac{kT}{q} \frac{Q_S - Q_D}{L} + \frac{Q_S^2 - Q_D^2}{2LC'_{\rm ox}} \right) \times (1 + \lambda (V_{\rm DS} - V_{\rm Dsat})) \quad (1)$$

where W is the channel width, L is the channel length, C'_{ox} is the unit-area gate-dielectric capacitance, λ is the channel-length modulation factor, and μ is the effective carrier mobility. Q_S and Q_D describe the density of quasi-mobile charges per gate area at the source and drain end of the channel, respectively, and can be expressed as

$$Q_{S,D} = \frac{S}{\ln(10)} C'_{\text{ox}} \mathcal{L}\left\{\exp\left(\frac{V_{\text{GS},D} - V_{T0}}{S/\ln(10)}\right)\right\}$$
(2)

where \mathcal{L} is the first branch of the Lambert W function, S is the subthreshold swing and V_{T0} is the threshold voltage.

The fluctuation of the drain-current around its nominal value is considered to be a result of the sum of all local fluctuation contributions along the channel. The transistor channel is divided into a noisy element between positions x and $x + \delta x$ and two noiseless pseudo-transistors T_1 and T_2 (Fig. 2) of channel lengths x and L - x, respectively. The local drain-current fluctuation is modeled as a current source δI_x connected in parallel to the resistance δR of the channel element. The term δI_x is considered to be a zero-mean stationary process on x. The equivalent small-signal circuits of transistors T1 and T2 can be reduced to the conductances G_1 and G_2 [10]. Consequently, the local current fluctuation is given by

$$\delta I_{xD} = G_{\rm CH} \,\delta R \,\delta I_x \tag{3}$$

where $G_{\rm CH} = G_{\rm CH}(x)$ is the conductance at point x of the channel. Moreover, $G_{\rm CH}$ and δR can be expressed as

$$G_{\rm CH} = \frac{dI_D}{dV} = \mu \frac{W}{L} \left(-Q_{\rm CH}\right) \tag{4}$$

and

$$\delta R = \frac{\delta V}{I_D} = \frac{\delta x}{W\mu(-Q_{\rm CH})} \tag{5}$$

respectively. By substituting (4) and (5) into (3) the following can be obtained:

$$\delta I_{xD} = \frac{\partial x}{L} \delta I_x. \tag{6}$$

Considering again the elementary section of the channel between x and $x + \delta x$, the current at position x is given by

$$I_D = WqN(x)\mu \frac{dV}{dx} \tag{7}$$

where $N(x) = Q_{CH}(x)/q$ is the number of charge carriers per unit area. Following [11], if a certain number of carriers get trapped at position x of the channel, the relative local current fluctuation can be described as

$$\frac{\delta I_x}{I_D} = \frac{\delta I_D(x)}{I_D} = \frac{\delta Q_{\rm CH}}{Q_{\rm CH}} + \frac{\delta \beta}{\beta} \tag{8}$$

where the term $\delta\beta/\beta$ describes the effect of charge trapping or edge effects [4] on $\beta = \mu C'_{ox}(W/L)$. Attributing all variations to charge trapping and following [11], based on Matthiessen's rule, the carrier mobility including the effect of the trapping mechanism can be expressed as

$$\frac{1}{\mu} = \frac{1}{\mu_0} + a_c Q_t \Leftrightarrow \mu = \frac{\mu_0}{1 + a_c Q_t \mu_0} \tag{9}$$

where $Q_t = -q N_t$ is the density of trapped charges and $a_c = \tilde{a_c}/q$ is the Coulomb scattering coefficient [12]. Using (9), the following can be obtained:

$$\frac{\delta\beta}{\delta Q_t} = -a_c \mu\beta \tag{10}$$

and the relative current fluctuation can be expressed as

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{Q_{\rm CH}} \frac{\delta Q_{\rm CH}}{\delta Q_t} - a_c \mu\right) \delta Q_t \tag{11}$$

where δQ_t is the local charge fluctuation related to the fluctuation in the trap density.

Considering that the variation δQ_t will cause a surfacepotential variation $\delta \psi_s$, the number of charges depending directly on ψ_s will also change. Consequently, the chargeconservation principle yields

$$-\delta Q_t = \delta Q_g + \delta Q_{\rm CH} \tag{12}$$

where δQ_g and δQ_{CH} are the induced fluctuations of charges on the gate electrode and of mobile charges in the channel, respectively. Furthermore, δQ_g and δQ_{CH} are related to the surface-potential variation $\delta \psi_s$ according to [13]

$$\delta Q_g = -C'_{\rm ox} \delta \psi_s, \ \delta Q_{\rm CH} = -C_{\rm CH} \delta \psi_s \tag{13}$$

where C_{CH} is the channel-charge capacitance. Recalling that C_{CH} can be approximated by

$$C_{\rm CH} \simeq -Q_{\rm CH}/U_T \tag{14}$$

where $U_T = kT/q$ is the thermodynamic voltage, and combining (12) and (13), the following can be obtained [13]:

$$\frac{\delta Q_{\rm CH}}{\delta Q_t} = \frac{C_{\rm CH}}{C_{\rm CH} + C'_{ox}}.$$
(15)

Using (14), (15) can be transformed into

$$\frac{\delta Q_{\rm CH}}{\delta Q_t} \simeq \frac{Q_{\rm CH}}{Q_{\rm CH} + Q^*/a} = \frac{q_{\rm ch}}{q_{\rm ch} + 1/a} \tag{16}$$

where $q_{\rm ch} = Q_{\rm CH}/Q^*$ is the normalized charge, $Q^* = -aU_T C'_{\rm ox}$ and $a = S/\ln(10)U_T$.

By substituting (16) into (11), the relative local current fluctuation can be rewritten as

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{q_{\rm ch} + 1/a} + a^*\mu\right) \frac{\delta Q_t}{Q^*} \tag{17}$$

where $a^* = a_c(-Q^*)$ is a parameter related to the Coulomb scattering coefficient given in units of $V \text{s/m}^2$.

Using (6), the mean square of the total drain-current fluctuation can be expressed as [10]

$$\sigma^{2}I_{D} = \overline{\delta I_{D}^{2}} = \sum_{L} \overline{\delta I_{xD}^{2}}$$
$$= \lim_{\delta x \to 0} \sum \overline{\left(\frac{\delta x}{L} \delta I_{x}\right)^{2}}$$
$$= \frac{1}{L^{2}} \int_{0}^{L} \delta x \overline{\delta I_{D}^{2}(x)} dx.$$
(18)

Furthermore, from (17), the relative local drain-current fluctuation normalized to the square of the drain current can be expressed as

$$\frac{\delta I_D^2(x)}{I_D^2} = \left(\frac{1}{q_{ch} + 1/a} + a^*\mu\right)^2 \frac{\delta Q_t^2}{Q^{*2}}.$$
 (19)

Following [10], the square of the standard deviation of the local fluctuations of the trap density, assuming a Poisson distribution, is given by

$$\sigma^2(\delta Q_t) = q^2 N_t / W \delta x \tag{20}$$

where N_t , given in units of m^{-2} , is the density of traps in which charge carriers may be accumulated and which will be treated as a fitting parameter. Combining (18)–(20), the variance of the total normalized drain-current fluctuation can be expressed as

$$\frac{\sigma^2 I_D}{I_D^2} = \frac{q^4 N_t}{W L^2 a^2 (kT)^2 C_{\text{ox}}^{\prime 2}} \int_0^L \left(\frac{1}{q_{\text{ch}} + 1/a} + a^* \mu\right)^2 dx \quad (21)$$

and by solving the integral, the following can be obtained:

$$\frac{\sigma^2 I_D}{I_D^2} = C^*|_{\Delta N} B^*(q_{ch})|_{\Delta N}$$
(22)

where

$$C^*|_{\Delta N} = \frac{q^4 N_t}{W L a^2 (kT)^2 C_{ox}^{/2}}$$
(23)

and

$$B^{*}(q_{s}, q_{d})|_{\Delta N} = \frac{1}{i_{d}} \left(\frac{2(a-1)a^{*}\mu}{a} + 1 \right) \ln \left(\frac{1+aq_{s}}{1+aq_{d}} \right) \\ + \frac{1}{i_{d}} \left(\frac{1-a}{1+aq_{s}} - \frac{1-a}{1+aq_{d}} \right) + (a^{*}\mu)^{2} \\ + \frac{1}{i_{d}} 2(a^{*}\mu)(q_{s} - q_{d}).$$
(24)



Fig. 3. Mean-value drain current $E[I_{DS}]$ versus gate–source voltage of coplanar DPh-DNTT TFTs with channel lengths (*L*) of 2, 3, and 5 μ m. Symbols: measurement data, solid lines: model.

The normalized drain current i_d can be expressed as $i_d = I_D/\mu (aU_T)^2 C'_{ox} W/L$. The terms $q_s = Q_S/Q^*$ and $q_d = Q_D/Q^*$ account for the normalized charge densities at the source and drain end of the channel, respectively. The impact of the parameter a^* is greatly reduced for gate–source voltages approaching the subthreshold region. Note that neither the current–voltage model nor the proposed variability model cover the OFF-state regime (leakage current region) below the turn-on (switch-on) voltage, i.e., the range of gate–source voltages between 0 and -0.5 V.

IV. RESULTS AND DISCUSSION

Fig. 3 shows the mean-value transfer characteristics of DPh-DNTT TFTs fabricated in the coplanar device architecture, having channel lengths (*L*) of 2, 3, and 5 μ m, for a drain–source voltage of -3.0 V. The experimental mean values were calculated over a population of 16 nominally identical TFTs fabricated on the same substrate. Symbols represent the measurement data and lines represent the results of the current–voltage model.

In Fig. 4(a)-(c), the normalized drain-current variance $\sigma^2 I_{\rm DS}/I_{\rm DS}^2$ of the coplanar DPh-DNTT TFTs is plotted as a function of the mean-value drain current $E[I_{DS}]$. The values of the parameters N_t and a^* were extracted as follows. In the first step, the parameter a^* was set to zero. In the subthreshold region, (i.e., above the leakage-current regime), a specific gate-source voltage was selected, and N_t at this gate-source voltage was calculated. In Fig. 4, the analysis was performed for a gate–source voltage of -0.7 V; black dashed lines show the results of the model without the mobility-fluctuation effect $(a^*\mu = 0)$. In the second step, using the extracted value of N_t , the parameter a^* was calculated at the maximum gate-source voltage, in our case $V_{GS} = -3.0$ V. Note that the two selected gate-source voltages, (subthreshold region and maximum $|V_{GS}|$) correspond to specific experimental values of $\sigma^2 I_{\rm DS}/I_{\rm DS}^2$ that define the subthreshold and maximum- $|V_{\rm GS}|$ asymptotes that are depicted in Fig. 4(a)-(c) as red dashed lines. To improve the agreement between model and experiment, the extraction of N_t and a^* was performed for each channel length individually as proposed in [10]. In Fig. 4(d), the standard deviation of the drain current normalized to the device area $\sigma(I_{\rm DS}/\rm WL)$ is plotted as a function of the gate–source voltage V_{GS} for the three different channel lengths.



Fig. 4. Normalized drain-current variance $\sigma^2 I_{\rm DS}/I_{\rm DS}^2$ versus mean-value drain current $E[I_{\rm DS}]$ of coplanar DPh-DNTT TFTs with (a) $L = 2 \ \mu$ m, (b) $L = 3 \ \mu$ m, and (c) $L = 5 \ \mu$ m. (d) Standard deviation of the drain current normalized to the device area $\sigma(I_{\rm DS}/WL)$ versus gate–source voltage of the same TFTs. The experimental mean values were calculated over a population of 16 nominally identical TFTs. Symbols: measurement data, black solid/dashed lines: model, red dashed lines: asymptotes.

In Fig. 5, the normalized drain-current variance multiplied by the square-root of the device area $\sigma^2 I_{\rm DS}/I_{\rm DS}^2 \times ({\rm WL})^{1/2}$ of the coplanar DPh-DNTT TFTs is plotted as a function of $1/({\rm WL})^{1/2}$. The dashed line is the result from the model calculated for $N_t = 6.9 \times 10^{18} \text{ m}^{-2}$ and $a^* = 750 \text{ vS/m}^2$.



Fig. 5. Normalized drain-current variance multiplied by the square-root of the device area $\sigma^2 I_{\rm DS}/I_{\rm DS}^2 \times ({\rm WL})^{1/2}$ versus $1/({\rm WL})^{1/2}$ of coplanar DPh-DNTT TFTs. Symbols: measurement data, solid lines: model (different set of parameters extracted per geometry), dashed line: model (one set of parameters extracted after simultaneously fitting the model to the three different geometries).

 TABLE I

 EXTRACTED PARAMETERS OF THE VARIABILITY MODEL

	$N_t ({\rm m}^{-2})$	$a^* (Vs/m^2)$	$\mu_{eff} (\mathrm{cm}^2/\mathrm{Vs})$
$L = 5 \mu \mathrm{m}$	1.5×10^{19}	625	3.3
$L = 3 \mu m$	7.5×10^{18}	850	3.0
$L = 2 \mu m$	$6.0 imes 10^{18}$	430	2.7
$L = 1 \mu m$	7.0×10^{17}	2380	1.4

This set of parameters was extracted by fitting the model to the experimental results obtained for each channel length. In this case, the model assumes the same value of N_t regardless of the channel length and predicts the number of traps ($N_t \times WL$) for each channel length, which yielded values of 1.73×10^9 , 6.21×10^8 and 2.76×10^8 for the TFTs having channel lengths of 5, 3, and 2 μ m, respectively. Using the alternative approach in which a different set of parameters N_t and a^* was extracted for each channel length, the predicted numbers of traps are 3.75×10^9 , 6.75×10^8 , and 2.40×10^8 for channel lengths of 5, 3, and 2 μ m, respectively. Both approaches correctly predict that the number of traps increases approximately linearly with the TFT area [14].

In Fig. 6(a) and (b), the results obtained for the staggered DNTT TFTs having a channel length of 1 μ m [8], are summarized. The values of the parameters N_t and a^* were extracted at gate–source voltages of -0.25 V (subthreshold region) and -2.0 V (maximum $|V_{GS}|$). The threshold voltage (V_{T0}) was found to be -0.33 V. Compared with the coplanar DPh-DNTT TFTs, the measured transfer characteristics of the DNTT TFTs show a larger OFF-state drain current (leakage) and a larger subthreshold swing, which prevent the formation of a clear plateau in the measured $\sigma^2 I_{DS}/I_{DS}^2$ curve.

Table I summarizes the values of N_t and a^* extracted from the variability model and the effective carrier mobilities of the coplanar DPh-DNTT TFTs and of the staggered DNTT TFTs for each channel length at the maximum gate–source and drain–source voltages. As can been seen, the value of a^* is significantly smaller for the coplanar DPh-DNTT TFTs than for the staggered DNTT TFTs. The reason is that the coplanar DPh-DNTT TFTs have a larger intrinsic channel mobility, a larger channel length and a smaller contact resistance than the staggered DNTT TFTs, all of which leads to a significantly



Fig. 6. (a) Normalized drain-current variance $\sigma^2 l_{\rm DS}/l_{\rm DS}^2$ versus mean-value drain current $E[l_{\rm DS}]$ of staggered DNTT TFTs with $L = 1 \ \mu m$. (b) Standard deviation of the drain current normalized to the device area $\sigma(l_{\rm DS}/WL)$ versus gate–source voltage of the same TFTs. Symbols: measurement data, black solid/dashed lines: model, red dashed lines: asymptotes.

larger effective carrier mobility [7], which in turn leads to a smaller value of a^* , in agreement with (9). In addition, the parameter a^* also accounts for the drain-current variability caused by edge effects [see (8)], and since these tend to be more pronounced in TFTs with a smaller area [4], the value of a^* is expected to increase with decreasing TFT area. The observation that the extracted effective carrier mobility of the DPh-DNTT TFTs decreases with decreasing channel length is consistent with the fact that the contribution of the contact resistance to the total device resistance increases with decreasing channel length [7]. The trap densities predicted by our model are smaller by three to four orders of magnitude than the trap density predicted in [4] for staggered DNTT TFTs with a channel length of 30 μ m and a channel width of 100 μ m (6.8 × 10²¹m⁻²), but larger by about two orders of magnitude than the trap densities reported in [14] for devices based on DNTT and DPh-DNTT (10^{16}m^{-2}) .

V. CONCLUSION

In conclusion, we have developed a physical charge-based drain-current variability model suitable for organic TFTs. The proposed model is based on charge-carrier-number-fluctuation and correlated-mobility-fluctuation effects and can be applied to TFTs fabricated in the coplanar or the staggered device architecture. We have shown that the drain-current variability decreases with increasing TFT area (product of channel length and channel width), particularly in the subthreshold region. We also found that the mobility-fluctuation effect is less pronounced in coplanar DPh-DNTT TFTs than in staggered DNTT TFTs and that the value of the parameter a^* tends to increase with decreasing channel length, due to the fact that a smaller channel length causes a smaller effective carrier mobility and more pronounced edge effects. Regardless of the channel dimensions and the device architecture, the results of the proposed model are in good agreement with the experimentally measured bias-dependent drain-current variability of organic TFTs.

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