# Three-Terminal Floating-Gate Cell for Threshold-Voltage Control of Organic Thin-Film Transistors

Kareem Mansour, Samar Elsaegh, Ute Zschieschang, Hagen Klauk, and Ghada H. Ibrahim

***Abstract*— A floating-gate (FG) cell as a circuit-level approach to control the threshold voltage of organic thin-film transistors (TFTs) operated in the transdiode configuration is presented. Charging and discharging of the FG are achieved by controlling the charge leakage through the gate dielectric of one of the organic TFTs that constitute the FG cell. Using programming voltages not exceeding 4 V, systematic tuning of the threshold voltage to values between −0.5 and 2.6 V was achieved. The versatility of the concept is demonstrated by employing organic-TFT-based FG cells as transdiodes with programmable threshold voltage in passive rectifiers and diode-load inverters fabricated on flexible, transparent plastic substrates. Rectifiers with programmable FG cells show flatter frequency response, improved 3-dB point, and reduced ripple compared to conventional rectifiers. Inverters with programmable FG-transdiode load have larger small-signal gain, larger output-voltage swing, and larger noise margins than conventional diode-load inverters.**

***Index Terms*— Diode-load inverters, floating-gate (FG) cells, organic thin-film transistors (TFTs), rectifiers, threshold-voltage control.**

## I. Introduction

ORGANIC thin-film transistors (TFTs) fabricated on plastic substrates offer a possible route for flexible electronics applications. While substantial progress has been made in the development of p-channel organic TFTs with low operating voltages, low contact resistance, large on/off ratios, long-term stability, small dimensions and high-frequency characteristics [1], [2], the performance and stability of n-channel organic TFTs are still notably inferior. Most organic circuits are thus designed as unipolar circuits based exclusively on p-channel TFTs [3], [4]. To obtain sufficient noise margins, this generally requires some form of threshold-voltage control [5], which is also useful for compensating device-to-device variations and uncontrolled threshold-voltage shifts caused by aging or bias stress [6]. Threshold-voltage control in organic TFTs is typically implemented through modifications to the TFT technology, e.g., by including an additional gate electrode, either in the form of a back gate [7] or as a programmable floating gate (FG) buried inside the gate dielectric [8]. One drawback of these approaches is that they require modifications to the TFT-manufacturing process. An alternative is to implement the functionality of the additional gate electrode outside of the transistor, e.g., by designing a three-terminal cell that consists of the transistor itself and one or more additional devices mimicking a programmable FG, so that the three-terminal FG cell emulates a TFT with built-in threshold-voltage control. This concept was initially developed for silicon CMOS [9] and is demonstrated here using organic TFTs. Each FG cell consists of three TFTs (two p-channel and one n-channel) that have their gate electrodes connected to each other (forming the FG) but not to a terminal of the cell. Charging and discharging of the FG are achieved by controlling the charge leakage through the gate dielectric of the n-channel TFT. The concept is demonstrated by employing FG cells as p-channel transdiodes with programmable threshold voltage in passive rectifiers and diode-load inverters.

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## II. Transistor Fabrication and FG-Cell Design

All TFTs and circuits were fabricated on polyethylene naphthalate (PEN) substrates by shadow-mask lithography using the process described in [10]. A schematic TFT cross section is shown in Fig. 1(a). The process includes the deposition of 30-nm-thick aluminum for the gate electrodes and 30-nm-thick gold for the source/drain contacts and the interconnects, including the connections between the gate electrodes of the TFTs. The gate dielectric is a stack of oxygen-plasma-grown aluminum oxide ($AlO_x$) and a molecular self-assembled monolayer (SAM) with a thickness of 6 nm, a unit-area capacitance of 0.6 $\mu$F/cm$^2$, and a leakage-current

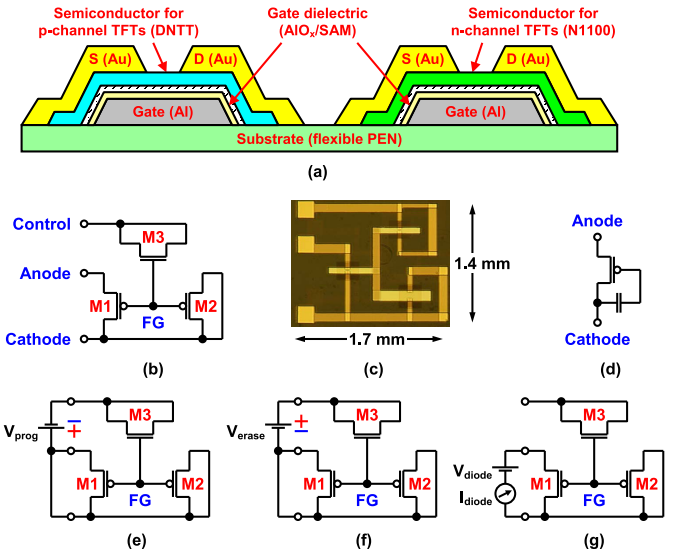


Fig. 1. FG cells fabricated using organic TFTs. (a) Schematic cross section of the organic TFTs. (b) Design, (c) photograph, and (d) circuit symbol of the FG cell. (e) Programming (charging) of the FG. (f) Erasing (discharging) of the FG. (g) Operation of the FG cell as a transdiode.

density of about $10^{-5}$ A/cm$^2$ at the voltages relevant here [11]. The vacuum-deposited small-molecule semiconductors dinaphtho[2,3-b:2',3'-f] thieno[3,2-b] thiophene (DNTT) and ActivInk N1100 were used for the p- and n-channel TFTs, respectively, [12]. All layers were patterned using polyimide shadow masks, except for the $AlO_x$/SAM gate dielectric that grows selectively on the aluminum gate electrodes.

The design, layout, and circuit symbol of the FG cell emulating a p-channel transistor with programmable threshold voltage are shown in Fig. 1(b)–(d). The cell consists of the p-channel TFT itself (M1), a capacitor as the FG (implemented using a p-channel TFT; M2), and a capacitor to program and erase the FG (implemented using an n-channel TFT; M3). The n-channel TFT provides a source of electrons to facilitate the negative charging of the FG to be able to shift the threshold voltage toward more positive values. Since the n-channel TFT is not in the signal path, its performance does not affect the circuit performance. M1 operates as a transdiode. M2 stores built-up charges, so its capacitance must be sufficiently large to facilitate efficient voltage division. In programming mode, M1, M2, and M3 form a capacitive voltage divider. Provided that the capacitance of M3 is small compared to the sum of the capacitances of M1 and M2, most of the programming voltage will drop across the gate dielectric of M3 to cause a large number of electrons to tunnel from the source/drain contacts of M3 to the FG. The dimensions of M3 are thus chosen to be as small as possible. The TFTs have the following channel lengths ($L$) and widths ($W$): M1: $L$ = 10 $\mu$m, $W$ = 60 $\mu$m; M2: $L$ = W = 60 $\mu$m; M3: $L$ = 10 $\mu$m, $W$ = 50 $\mu$m. All three TFTs have gate-to-source and gate-to-drain overlaps of 30 $\mu$m. The FG cell occupies an area of 1.7 mm × 1.4 mm.

## III. FG Cells as Transdiodes

In the following, the behavior of the FG cell is demonstrated by operating it as a p-channel transdiode. Since the p-channel

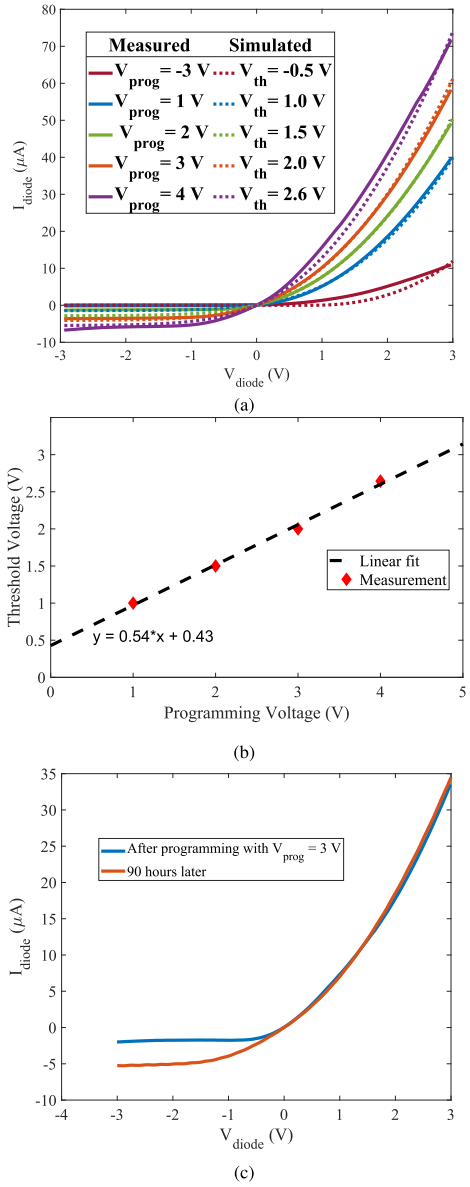


Fig. 2. (a) Measured (lines) and simulated (symbols) current–voltage characteristics of an FG cell operated as a transdiode ($I_{diode}$–$V_{diode}$). Each curve was recorded in a three-step procedure by discharging the FG with an erase voltage ($V_{erase}$) of 3 V, charging the FG with a programming voltage ($V_{prog}$) of 0, 1, 2, 3, or 4 V, and operating the FG cell as a transdiode by measuring the current ($I$) as a function of voltage ($V$). (b) Dependence of the threshold voltage of the transdiode on the programming voltage. (c) Measured charge-retention characteristics.

TFTs originally have a negative threshold voltage (−0.5 V), a shift of the threshold voltage toward more positive values by controlled charging of the FG with electrons supplied by M3 will lead to a notable improvement of the transdiode performance.

Programming (charging) and erasing (discharging) of the FG were performed by controlling the leakage current flowing from the source/drain contacts of M3 onto the FG. To charge the FG, the source and drain contacts of M1 (anode and cathode of the FG cell) were shorted and connected to the positive programming voltage $V_{prog}$, as shown in Fig. 1(e). Depending on the magnitude of $V_{prog}$, electrons leak from the source/drain

TABLE I
ORGANIC-TFT PARAMETERS EXTRACTED AND EMPLOYED FOR THE CIRCUIT SIMULATIONS

| Parameters | Units | Value | Parameter | Unit | Value |
|---|---|---|---|---|---|
| $\mu_o$ | [cm$^2$/Vs] | 0.9 | $V_{th}$ | [V] | -0.5 |
| $C_{diel}$ | [μF/cm$^2$] | 0.7 | $W_{fringe}$ | [μm] | 10 |
| $V_T$ | [mV] | 25.9 | $J_{os}$ | [A/m$^2$] | 750 |
| $\eta_s$ | - | 21.45 | $P_{snorm}$ | - | 0.8 |
| $J_{od}$ | [A/m$^2$] | 27250 | $\eta_d$ | - | 4 |
| $P_{dnorm}$ | - | 0.8 | | | |

contacts of M3 onto the FG, which produces an effect similar to a shift of the threshold voltage of M1 toward more positive values. To discharge the FG, a negative erase voltage $V_{erase}$ is applied, as shown in Fig. 1(f). After disconnecting M3, the FG cell can then be operated as a transdiode, with the voltage being applied between the source and drain terminals of M1, denoted by ($V_{diode}$), drawing current ($I_{diode}$), as shown in Fig. 1(g).

The measured and simulated current–voltage characteristics of the FG cell when operated as a transdiode following erasing and programming with different programming voltages are shown in Fig. 2(a). Each of the current–voltage curves in Fig. 2(a) was recorded in a three-step procedure. First, the FG was discharged by applying an erase voltage ($V_{erase}$) of $-3$ V for a period of 60 s. Second, the FG was charged by applying a programming voltage ($V_{prog}$) of 1, 2, 3, or 4 V for a period of 60 s (or by not applying a programming voltage at all, labeled as "$V_{prog} = 0$ V in Fig. 2(a)." Finally, the FG cell was operated as a transdiode, as shown in Fig. 1(g), by measuring the current ($I$) as a function of the applied voltage ($V$). From Fig. 2(a), the equivalent threshold voltages of $-0.5$, 1.0, 1.5, 2.0, and 2.6 V are extracted after programming the FG cell with the programming voltages of 0, 1, 2, 3, and 4 V, respectively; these values are also summarized in the legend in Fig. 2(a). Simulations were performed using a compact dc model [13], and the parameters extracted for the p-channel DNTT TFTs are summarized in Table I. By performing the simulations using the threshold voltages extracted from Fig. 2(a), good agreement between measurement data and simulation results was achieved for each programming voltage, indicating successful programming of the FG cell. The discrepancies observed between the measured and simulated current–voltage curves for the programming voltages of 0 and 4 V are ascribed to photocurrents and onset of dielectric breakdown, respectively. Fig. 2(b) shows that the dependence of the threshold voltage on the programming voltage is approximately linear, with a slope of 0.5.

The charge-retention characteristics of the FG cell are shown in Fig. 2(c). For these measurements, the FG was discharged with an erase voltage of $-3$ V and then charged with a programming voltage of 3 V. The current–voltage characteristics were then measured immediately after programming and again four days later. As can be seen, the difference in the forward currents measured immediately after programming and four days later is very small, only about 4%. There is, however, a significant increase in the leakage

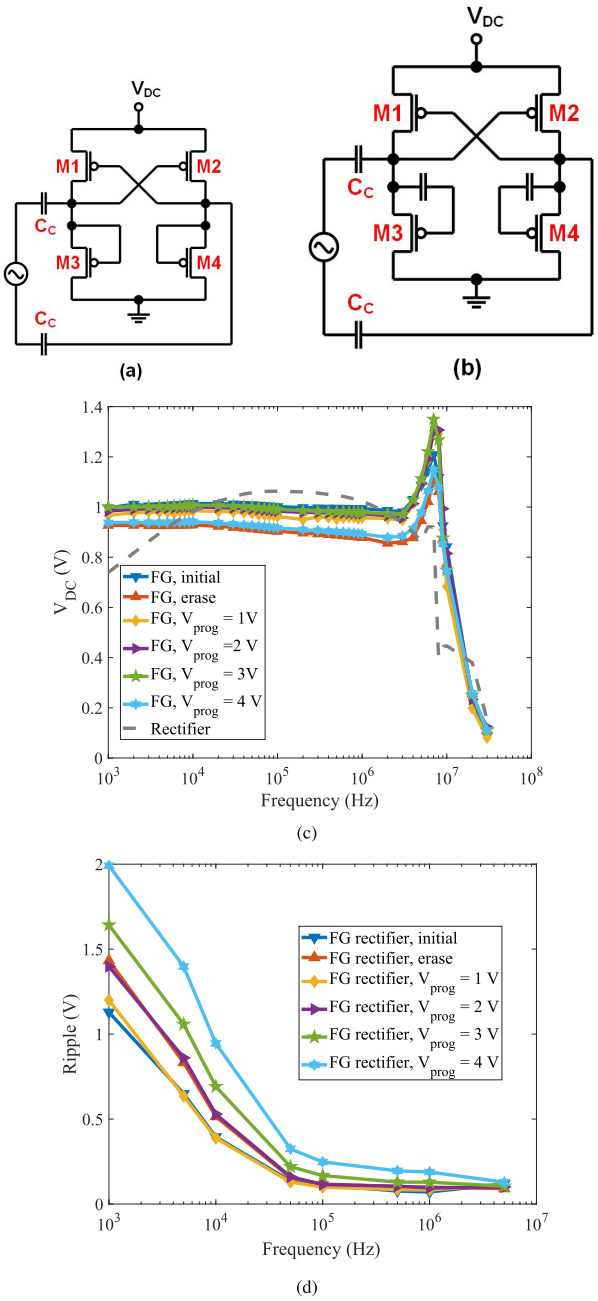


Fig. 3. Differential rectifiers with dynamic-threshold-voltage compensation. (a) Circuit diagram when M3 and M4 are implemented as diode-connected transistors. (b) Circuit diagram when M3 and M4 are implemented as FG cells. (c) DC output voltage of both circuits measured for a sinusoidal input voltage with an amplitude of 2 V. For the circuit in which M3 and M4 were implemented as FG cells, the measurements were performed after the FG had been charged with programming voltages ($V_{prog}$) of 0, 1, 2, 3, or 4 V. (d) Output ripple as a function of frequency. The four TFTs M1–M4 have the channel length of 10 $\mu$m and the channel width of 200 $\mu$m. FG cells are sized accordingly.

(reverse) current, the cause of which will require further investigation.

## IV. FG RECTIFIERS

The design of efficient rectifiers would benefit from the availability of high-quality Schottky diodes [14]. Both in silicon CMOS and in flexible organic electronics, the lack

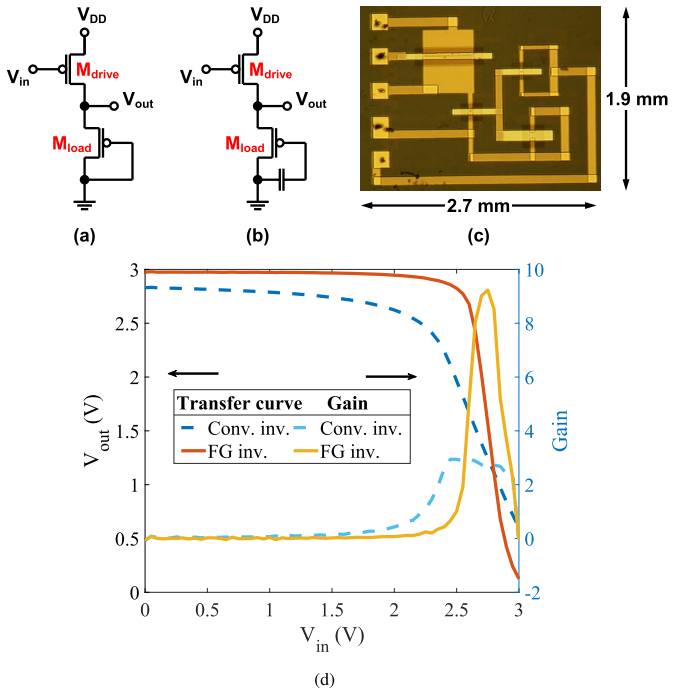


Fig. 4. Inverters with transdiode load. (a) Circuit diagram of a conventional diode-load inverter. (b) Circuit diagram of the proposed FG-transdiode-load inverter. (c) Photograph of the proposed FG-transdiode-load inverter. (d) Transfer characteristics of both inverters measured for a supply voltage of 3 V. In the case of the inverter with the FG-transdiode load, the measurement was performed after the FG had been charged with a programming voltage ($V_{prog}$) of 3 V. $M_{drive}$ has a channel length of 10 $\mu$m and a channel width of 600 $\mu$m; all other dimensions are identical to those in Fig. 1 (a) (d).

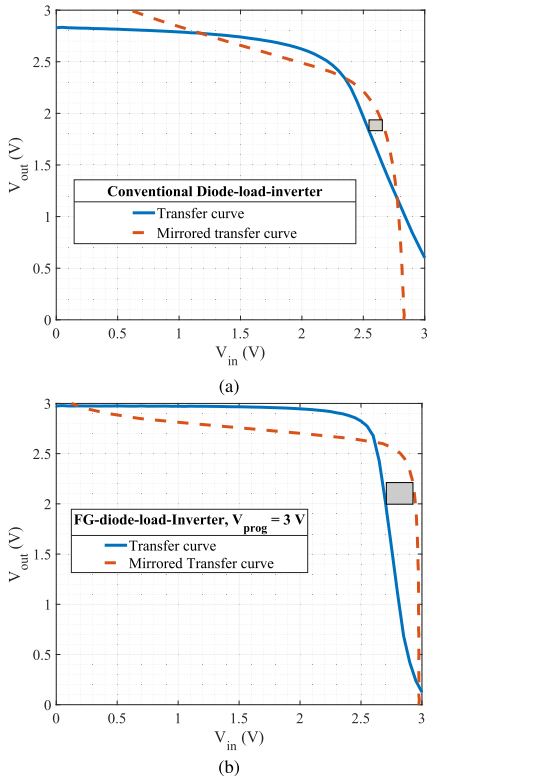


Fig. 5. Evaluation of the noise margins of (a) conventional diode-load inverter and (b) proposed FG-transdiode-load inverter.

of such diodes is compensated for by the use of diode-connected transistors (transdiodes). This necessitates some form of threshold-voltage compensation to account for the higher threshold voltage of rectifiers based on transdiodes, compared to rectifiers based on Schottky diodes. An example is dynamic threshold-voltage cancellation, which minimizes the effective threshold voltage in the forward direction while maximizing it in the reverse direction for reduced leakage. This concept was initially proposed for silicon CMOS technology [9], [15] and recently demonstrated with organic TFTs [16]. The circuit diagram of a single-stage differential-drive dynamic-threshold-voltage-compensated rectifier implemented using organic TFTs is shown in Fig. 3(a).

By replacing the diode-connected M3 and M4 in Fig. 3(a) with FG cells, as shown in Fig. 3(b), the threshold voltage can be further reduced. Fig. 3(c) shows the dc output voltage of both circuits measured for a sinusoidal input voltage with an amplitude (peak-to-peak voltage $V_{pp}$) of 2 V and frequencies ranging from 1 kHz to 30 MHz. For the circuit in which M3 and M4 were implemented as FG cells, the measurements were performed after the FGs had been charged with programming voltages ($V_{prog}$) of 0, 1, 2, 3, or 4 V. In Fig. 3(d), the ripple is plotted as a function of frequency. The only smoothing capacitors are the parasitic capacitance inherent to the circuit layout with a value of 100 pF and the capacitance of the measurement equipment with a value of 13 pF for both circuits in Fig. 3(a) and (b). Comparing the results obtained for the two circuits, the circuit in Fig. 3(b) provides a flatter frequency response and an improved 3-dB point. The best compromise between dc output voltage and ac ripple is obtained for a programming voltage ($V_{prog}$) of 1 V. Larger programming voltages cause a shift of the threshold voltage of M3 and M4 to positive values, resulting in excessive leakage and greater ripple.

## V. Programmable Diode-Load Inverters

Unipolar logic gates require load devices, the design of which often involves compromises between the various static and dynamic inverter-performance characteristics. Load designs for unipolar logic include the transdiode load [see Fig. 4(a)], the zero-gate-source voltage (VGS) load, and the biased load; examples for more complex designs include the pseudo-CMOS and the bootstrap designs [3], [5], [7], [17]–[19]. Replacing the conventional transdiode load with an FG cell makes it possible to control the threshold voltage of the load and to switch it between enhancement- and depletion-mode behavior, with the potential of alleviating some of the compromises between the inverter parameters.

The circuit diagram of a conventional diode-load inverter is shown in Fig. 4(a); the circuit diagram and the layout of the proposed FG-transdiode-load inverter are shown in Fig. 4(b). Transistor M1 in the FG cell that constitutes the load transistor $M_{load}$ of the inverter has a channel width of 60 $\mu$m, while the drive transistor $M_{drive}$ has a channel width of 600 $\mu$m. Both have a channel length of 10 $\mu$m. Fig. 4(c) shows the measured transfer characteristics of a conventional diode-load inverter and the proposed FG-transdiode-load inverter. For the latter, the measurement was performed after charging the FG with a programming voltage ($V_{prog}$) of 3 V. Comparing the results

obtained for the two inverters, the proposed FG-transdiode-load inverter provides a larger output–voltage swing (2.8 V versus 2.1 V) and a higher small-signal gain (9 instead of 3). The evaluation of the noise margins of both inverters according to the maximum equal criterion [3], [5] is shown in Fig. 5, yielding the noise margins of 100 and 200 mV for the conventional inverter and the proposed FG-transdiode-load inverter, respectively.

## VI. Conclusion

A circuit-level approach for controlling the threshold voltage of organic TFTs operated in the transdiode configuration has been presented. Rather than modifying the transistor structure, the functionality of an FG is implemented by using two additional TFTs so that the resulting three-terminal FG cell emulates an organic-TFT-based transdiode with built-in threshold-voltage control. The penalty compared to circuits based on transistors with a built-in additional gate electrode is a larger circuit area, which is acceptable for large-area application scenarios. The ability to control the threshold voltage of organic TFTs may also be useful to counteract device degradation caused by aging and bias stress.

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