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Noise-Based Simulation Technique for Circuit-Variability Analysis

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ABSTRACT An accurate and efficient noise-based simulation technique for predicting the impact of device-parameter variability on the DC statistical behavior of integrated circuits is presented. The proposed method is validated on a source follower, a diode-load inverter and a current mirror based on organic thin-film transistors. Taking advantage of the standard noise analysis of a circuit, after translating the statistical variation of the electrical parameters of the transistors into equivalent-noise circuit components, the proposed technique yields results identical to those obtained from a Monte Carlo simulation, but in a significantly shorter amount of time.

INDEX TERMS Variability, noise, Monte Carlo analysis, compact modeling, verilog-A, thin-film transistor, organic circuits.

I. INTRODUCTION

Parameter variability can be perceived as statistical fluctuations in the values of the electrical parameters of electronic devices. In the case of field-effect transistors, this includes fluctuations in the threshold voltage, the charge-carrier mobility and the channel dimensions [1], [2]. The impact of transistor-parameter variability on the performance of integrated circuits is usually predicted by Monte Carlo (MC) simulations [3]. As an alternative, a noise-based simulation technique initially introduced in [4] with the name "Noise Based Variability Approach" (NOVA) is presented here. The proposed method is suitable for commercial electronic device automation (EDA) software tools and is expected to accelerate the process of approximating the influence of parameter variability on integrated circuits.

Organic thin-film transistors (TFTs) are field-effect transistors in which the semiconductor is a thin, usually polycrystalline layer of conjugated organic molecules [5]. Organic TFTs are typically processed at temperatures below 100 °C [6] and can therefore be useful for a variety of large-area flexible electronics applications [7]. The statistical analysis of organic TFT-based circuits is typically performed using either Monte Carlo simulations (similar to those developed for silicon-CMOS circuits) [8] or novel physics-based variability compact models (which were developed to accurately describe the drain-current variability in organic TFTs) [9]. Here, the proposed NOVA method [4] is validated for a number of organic-TFT-based circuit topologies.

The context of this article is organized as follows. Section II describes the technology of the organic-TFTs used for verification. Section III summarizes the compact model used for the simulations. In Section IV the typical Monte Carlo analysis performed using Cadence Virtuoso ADE and Spectre simulator framework [10] is presented. The proposed NOVA method is analytically explained in

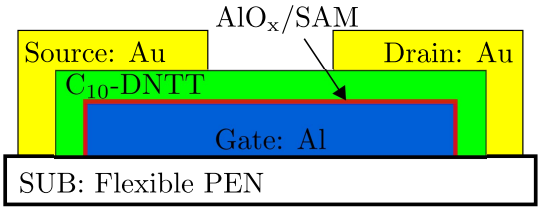

FIGURE 1. Schematic cross-section of the organic TFTs fabricated in the inverted staggered (bottom-gate, top-contact) architecture [11].

Section V. Section VI includes the results of the current analysis. In Section VII conclusions are drawn.

II. DEVICES AND MEASUREMENTS

The experimental population comprises 16 nominally identical p-channel organic TFTs having a nominal channel length (L) of 1 µm and a nominal channel width (W) of 10 µm. The TFTs were fabricated on a flexible polyethylene naphthalate (PEN) substrate with a thickness of 125 µm in the inverted staggered (bottom-gate, top-contact) device architecture, using stencil lithography based on high-resolution silicon stencil masks (Fig. 1) [11]. The TFTs consist of 20-nm-thick aluminum gate electrodes, a 5.3-nm-thick hybrid AlO_x/SAM gate dielectric, 20-nm-thick gold (Au) source and drain contacts and a 20-nm-thick vacuum-deposited layer of the small-molecule semiconductor 2,9-didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (C_{10}-DNTT). The maximum process temperature was 90 °C. The transfer characteristics of all TFTs were recorded at room temperature by applying a drain-source voltage (V_{DS}) of −2.0 V and sweeping the gate-source voltage (V_{GS}) from 0 to −2.0 V with a step size of −25 mV.

III. COMPACT MODELING

In this section, the core of the simulation, namely the application of a compact model to the measured current-voltage characteristics, will be described. The charge-based organic-TFT model presented in [12] will be used as the basis. The proposed current-voltage model provides a single current equation valid for all operation regions that can be obtained from

$$I_{DS} = \mu_{eff} W \left(\frac{kT}{q} \frac{Q_S - Q_D}{L} + \frac{Q_S^2 - Q_D^2}{2LC'_{ox}} \right) \times (1 + \lambda(V_{DS} - V_{Dsat})), \quad (1)$$

where W is the channel width, L is the channel length, C'_{ox} is the unit-area gate-dielectric capacitance, λ is the channel-length modulation factor and μ_{eff} is the effective carrier mobility.

Q_S and Q_D describe the density of quasi mobile charges per gate area at the source and drain end of the channel respectively and can be expressed as

$$Q_{S/D} = \frac{S}{\ln(10)} C'_{ox} \mathcal{L} \left\{ \exp\left(\frac{V_{GS/D} - V_{T0}}{S/\ln(10)} \right) \right\}, \quad (2)$$

TABLE 1. Parameter variations of the extracted model cards.

	μ model	$\mu - \sigma$ model	$\mu + \sigma$ model	variation ×%
$vt0$	−333 mV	−363 mV	−304 mV	≃ ±8.7%
lch	1 µm	1.023 µm	0.975 µm	≃ ±2.5%

TABLE 2. Current variation of the extracted model cards.

	μ model	$\mu \pm \sigma$ model variation ×%
I_{vt0}	-1.49×10^{-8} A	≃ ±32%
I_{ON}	-9.39×10^{-6} A	≃ ±6%

where $\mathcal{L}$ is the first branch of the Lambert W function, S is the subthreshold swing and V_{T0} is the threshold voltage. The compact model is available in Verilog-A.

The process of extracting the variability-aware parameter set using the compact model is described in the following. First, the mean-value μ and the corner-value $\mu \pm \sigma$ transfer characteristics were acquired from the experimental current-voltage curves by calculating the sample-mean $E[I_{DS}]$ and the sample-standard-deviation $\sigma(I_{DS})$ of the drain current I_{DS} at each gate-source voltage step. Next, one parameter set determining the mean-value model card was produced by fitting the compact model to the measured mean-value transfer characteristic. For the derivation of the $\mu \pm \sigma$ parameter sets, the mean-value model card was used as the basis, and a subset of newly adjusted parameters was obtained from the $\mu \pm \sigma$ experimental transfer characteristics using the fitting procedure. Specifically, the values of the Verilog-A parameters $vt0$ and lch that correspond to the threshold-voltage (V_{TO}) and the channel-length (L) parameters of (1) and (2), respectively, where varied accordingly. The variability of the drain current in the subthreshold region can be attributed to the variation of the threshold voltage. In addition, the channel-length variation caused by edge effects [13] impacts the saturation current linearly in the above-threshold regime [3]. The parameters $vt0$ and lch are considered to be statistically independent.

In Fig. 2(a), the experimental transfer characteristics of the 16 nominally identical p-channel C_{10}-DNTT TFTs are depicted as black lines. Fig. 2(b) shows the μ and $\mu \pm \sigma$ transfer characteristics of the same TFTs. Symbols denote the measurements, and lines correspond to the simulation results calculated from the three different model cards. Tables 1 and 2 summarize the values and variations of the parameters $vt0$ and lch and the drain-current variation of the extracted model cards, respectively. I_{vt0} and I_{ON} are the simulated drain currents at the threshold voltage and at the maximum gate-source voltage, respectively.

IV. TYPICAL MONTE CARLO ANALYSIS

The Monte Carlo analysis is a popular approach to determine the statistical distribution of the performance of integrated circuits. It consists of a sequential number of simulations in which for each iteration, the values of a parameter subset of a particular circuit component are randomly varied and the circuit is simulated accordingly. Subsequently, the statistical results are collected and the yield of the examined circuit

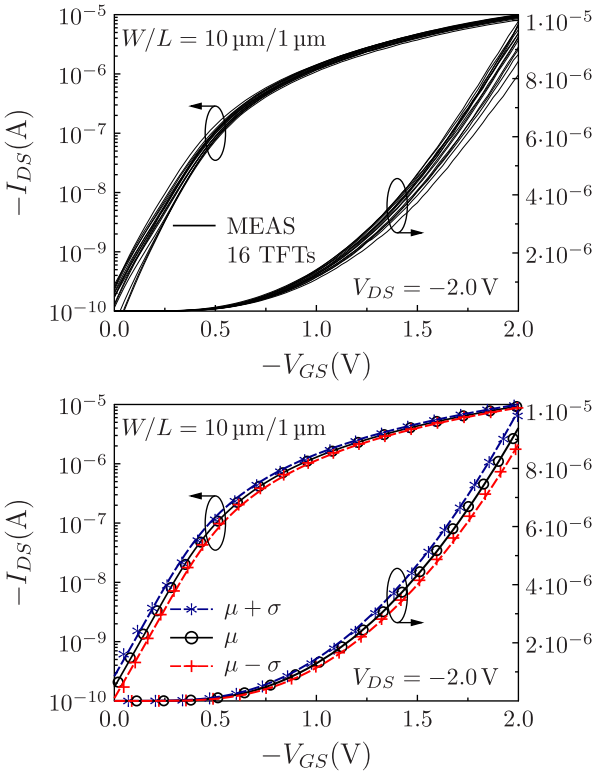

FIGURE 2. **(a) Measured transfer characteristics of the 16 nominally identical p-channel C_{10}-DNTT TFTs ($W = 10\,\mu m$, $L = 1\,\mu m$) in the saturation regime (black lines). (b) μ and $\mu \pm \sigma$ transfer characteristics of the same TFTs. Symbols: Values calculated from measurements. Lines: Simulation results calculated from the three different model cards.**

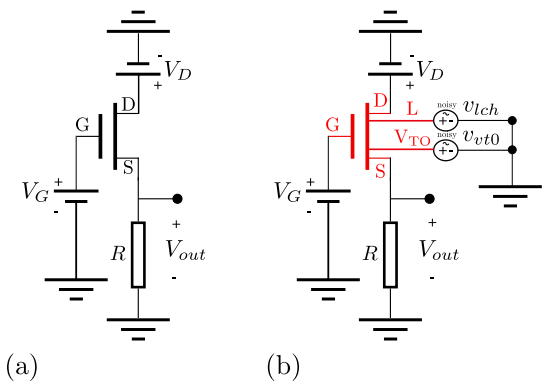

FIGURE 3. **(a) Schematic of a source follower comprising an instance of a Verilog-A three-terminal p-channel organic TFT, two DC voltage sources and an output resistor $R = 1\,\Omega$. (b) Same circuit topology as in (a) with the difference that the transistor instance is replaced by a five-terminal organic-TFT structure, with the two additional terminals connected to alternating "noisy" voltage sources in order to modify the Verilog-A parameters threshold voltage (*vt0*) and channel length (*lch*) according to the proposed NOVA method. All simulations are performed in Cadence Virtuoso ADE [10].**

is estimated. To achieve sufficient accuracy, the statistical Monte Carlo analysis of a circuit requires a sufficiently large number of iterations.

Fig. 3(a) shows the circuit schematic of a source follower designed for the Monte Carlo analysis to evaluate the impact

```
simulator lang=spectre
parameters vt0_stat =-0.333
parameters lch_stat =1e-6
statistics {
process {
vary vt0_stat dist=gauss std=8.7 percent=yes
vary lch_stat dist=gauss std=2.5 percent=yes } }
```

(a)

```
(*cds_inherited_parameter*)parameter real vt0_stat=0;
(*cds_inherited_parameter*)parameter real lch_stat=0;
localparam real vt0_var=vt0_stat+vt0;
localparam real lch_var=lch_stat+lch;
```

(b)

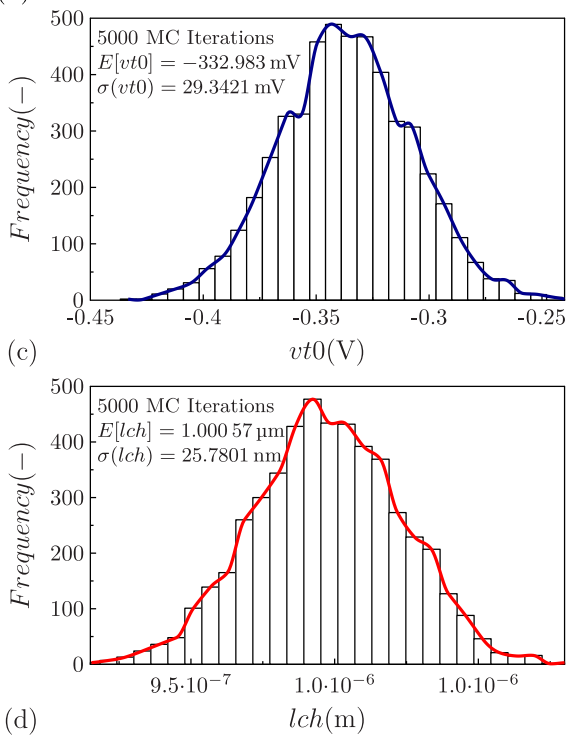

FIGURE 4. **(a) Library ".scs" file and (b) Verilog-A part of the source code used for the Monte Carlo analysis. (c), (d) Histograms of the statistical variations of the Verilog-A model parameters threshold voltage *vt0* and channel length *lch* after a Monte Carlo simulation with 5000 iterations.**

of process variability on the experimental performance of the p-channel C_{10}-DNTT TFTs. This source follower consists of a three-terminal Verilog-A p-channel organic TFT, two DC voltage sources and a "dummy" resistor $R = 1\,\Omega$. The TFT instance is configured with the parameter values of the mean-value (μ) model card. The resistance of the resistor was chosen to create zero effect on the simulated values of the drain current I_{DS}. Fig. 4(a) shows the custom ".scs" library file that is used for the interaction between the simulator and the TFT instance during the Monte Carlo analysis. In the "process" section of the source code, the parameters that are of statistical interest are listed. For each parameter, the distribution type and the deviation with respect to its mean value are determined. Specifically, both parameters have a Gaussian distribution, and their standard deviations

are assigned in percent. The numerical values of the simulation set-up are derived from the results listed oi Table 1. It has to be mentioned that the actual parameters *vt*0 and *lch* of the Verilog-A TFT instance of the circuit are affected during the Monte Carlo iterations via the variation of the parameters *vt*0_*stat* and *lch_stat*, respectively (Fig. 4(b)).

Figs. 4(c) and (d) show the derived Gaussian-shaped histograms of the statistical variations of the Verilog-A parameters threshold voltage (*vt*0) and channel length (*lch*) after a Monte Carlo simulation with 5000 iterations. The estimated mean values ($E[vt0]$, $E[lch]$) and the standard deviations ($\sigma(vt0)$, $\sigma(lch)$) are included in Figs. 4(c) and (d), and they are in very good agreement with the experimental results (Table 1).

V. NOISE-BASED VARIABILITY APPROACH (NOVA)

In this section, an alternative to the Monte Carlo simulation method that is capable of fast DC statistical evaluation of integrated circuits will be discussed. The proposed technique, namely "Noise-Based Variability Approach" (NOVA) [4], is based on noise-simulation principles and is validated here for organic-TFT-based circuit topologies, although it can be expanded to circuits based on silicon MOSFETs or inorganic TFTs.

In simulator-based noise analyses, the input of the circuit is connected to ground and the spectra of all noise-contributing circuit components are added to calculate the output signal. The result corresponds to the variance of the output signal. In Cadence [10] simulators, similar to other EDA software tools, a "noisy" voltage source can be implemented in the form of an AC voltage source instance representing the desired mean-square value of noise. In this way, a thermal-noise Thévenin equivalent circuit is implemented. The central-limit theorem indicates that thermal noise is Gaussian distributed with zero mean [14]. Furthermore, for Gaussian-distributed noise, the standard deviation σ is equal to the root-mean-square value of noise [15].

In Fig. 3(b), the schematic of the source follower used to evaluate the proposed NOVA method is depicted. The NOVA circuit topology is identical to the one that was used for the Monte Carlo analysis, with the difference that the transistor instance is replaced by a five-terminal organic-TFT structure. The two additional terminals are connected to alternating "noisy" voltage sources in order to modify the numerical values of the Verilog-A parameters threshold voltage (*vt*0) and channel length (*lch*). The setup of each additional voltage source is described next. The DC voltage and the mean-square values of noise are configured to be equal to the mean value and the variance of the targeted Verilog-A parameter, respectively. The Verilog-A code of the TFT instance is updated accordingly. Note that the number of additional terminals depends on the number of Verilog-A parameters of statistical interest (i.e., two in our case). After the circuit has been properly configured, a parametric noise analysis with respect to the different gate-source voltage bias points is performed. The result corresponds to the variance of the output signal.

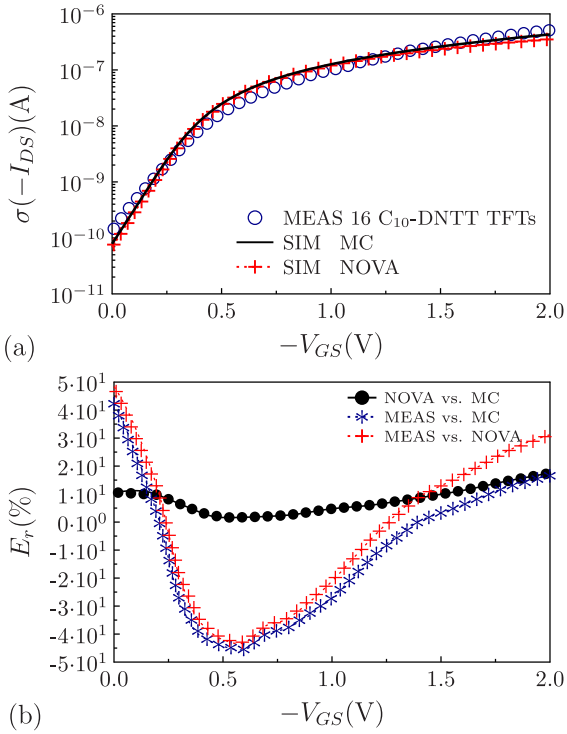

FIGURE 5. (a) Standard deviation of the output current $\sigma(-I_{DS})$ of the source follower of Fig. 3 as a function of the gate-source voltage V_{GS}. Blue circles: Measurements. Black line: Monte Carlo simulation with 5000 iterations. Red crosses: Proposed method (NOVA). (b) Relative errors.

VI. RESULTS AND DISCUSSION

Fig. 5(a) shows the standard deviation of the output current $\sigma(-I_{DS})$ of the source follower (Figs. 3(a), (b)). The blue circles indicate the result derived from the measurements, the black line indicates the prediction from a Monte Carlo simulation with 5000 iterations, and the red crosses account for the standard deviation of the drain current estimated using the proposed NOVA method. Both simulation methods are able to coherently describe the circuit-bias-dependent process variability and predict the same trends with regard to the gate-source voltage; Fig. 5(b) shows that the deviation between the results from the two methods is approximately 10 % across the full range of gate-source voltages.

In Fig. 7, the use of the proposed NOVA method for the variability study of an organic-TFT-based diode-load inverter is presented. The circuit (Fig. 6(a)) consists of a drive TFT (T1) and a load TFT (T2) to implement the pull-up and pull-down functionalities, respectively. For simplicity, both TFTs are designed to have the same channel dimensions as the experimental TFTs ($W = 10\,\mu$m, $L = 1\,\mu$m). For circuits that consist of more than one transistor, the simulator permits both process and mismatch Monte Carlo statistical analyses. In order to extend this ability to the NOVA method, the NOVA mismatch analysis is performed using different noisy

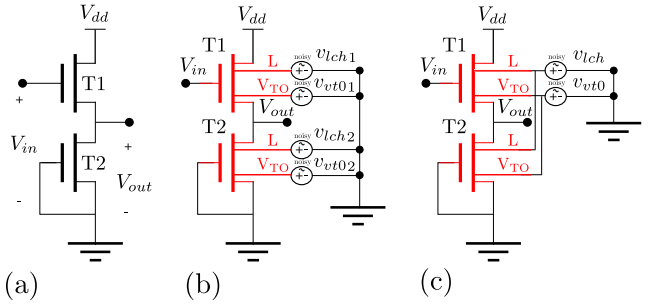

FIGURE 6. **(a) Schematic of a diode-load inverter used for Monte Carlo simulation. The topology is based on two identical p-channel TFTs ($W = 10\,\mu$m, $L = 1\,\mu$m) operated with a supply voltage $V_{dd} = 2.0$ V. Schematics of the same circuit designed for (b) the NOVA mismatch and (c) the NOVA process-variation analyses.**

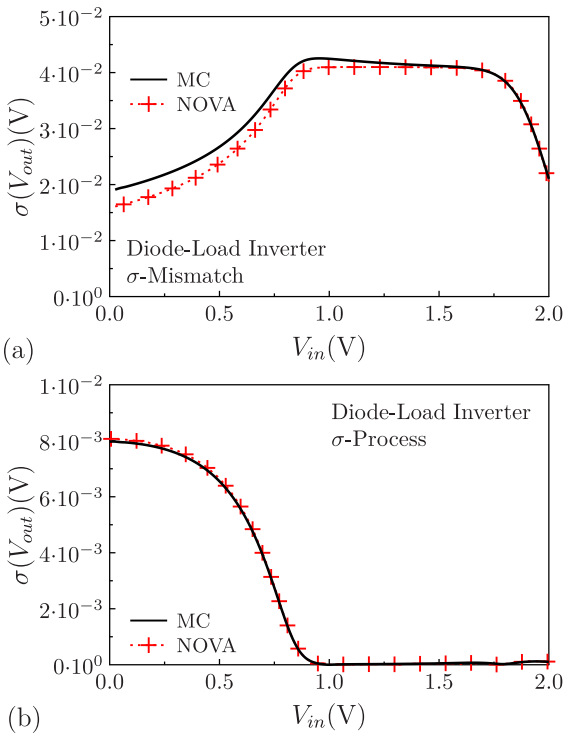

FIGURE 7. **Standard deviation of the output voltage $\sigma(V_{out})$ of the diode-load inverter of Fig. 6 as a function of the input voltage (V_{in}) for (a) mismatch and (b) process variations. Black line: Monte Carlo simulation with 5000 iterations. Red crosses: Proposed method (NOVA).**

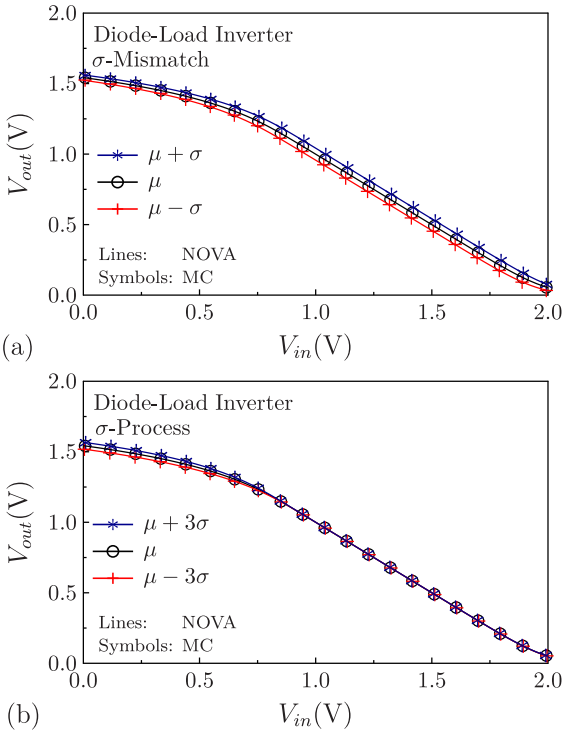

FIGURE 8. **Mean-value μ and corner-value $\mu \pm \sigma$ ($\mu \pm 3\sigma$) transfer characteristics of the diode-load inverter of Fig. 6 for (a) mismatch and (b) process variations. Symbols: Monte Carlo simulation with 5000 iterations. Lines: NOVA method.**

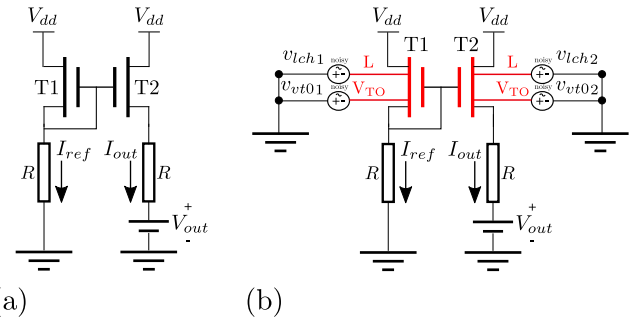

FIGURE 9. **(a) Schematic of a current mirror, used for Monte Carlo simulation, based on two identical p-channel TFTs ($W = 10\,\mu$m, $L = 1\,\mu$m) and two load resistors ($R = 1\,\Omega$) operated with a supply voltage (V_{dd}) of 2.0 V. (b) Schematic of the same circuit used for the NOVA mismatch variation analysis.**

voltage sources for transistors T1 and T2 (Fig. 6(b)), while for the NOVA process-variations analysis, the same noisy voltage source was used for all TFTs (Fig. 6(c)). In both cases, the Verilog-A parameters *vt*0 and *lch* of the TFTs where statistically varied according to Table 1. Figs. 7(a) and (b) show the estimated standard deviation $\sigma(V_{out})$ of the transfer characteristics for both the mismatch and the process analyses. In Figs. 8(a) and (b), the MC-versus-NOVA mean-value μ and corner-value $\mu \pm \sigma$ ($\mu \pm 3\sigma$ for process-variation-analysis) transfer characteristics are depicted. In all cases, the NOVA method accurately predicts the results of a Monte Carlo simulation with 5000 iterations.

A current mirror based on two identical p-channel TFTs ($W = 10\,\mu$m, $L = 10\,\mu$m) is depicted in Fig. 9(a). Both the reference TFT and the mirror TFT are connected to a load resistor ($R = 1\,\Omega$). In the basic DC simulation, the output voltage V_{out} was swept from zero to V_{dd}, and the output current I_{out} was recorded. Fig. 10(a) shows the standard deviation $\sigma(I_{out})$ of the output current, estimated after a NOVA-mismatch analysis (red crosses). The results are identical to those obtained using a Monte Carlo mismatch analysis with 5000 iterations (black line). The mean-value μ and the corner-value $\mu \pm \sigma$ output currents of the same circuit are shown in Fig. 10(b).

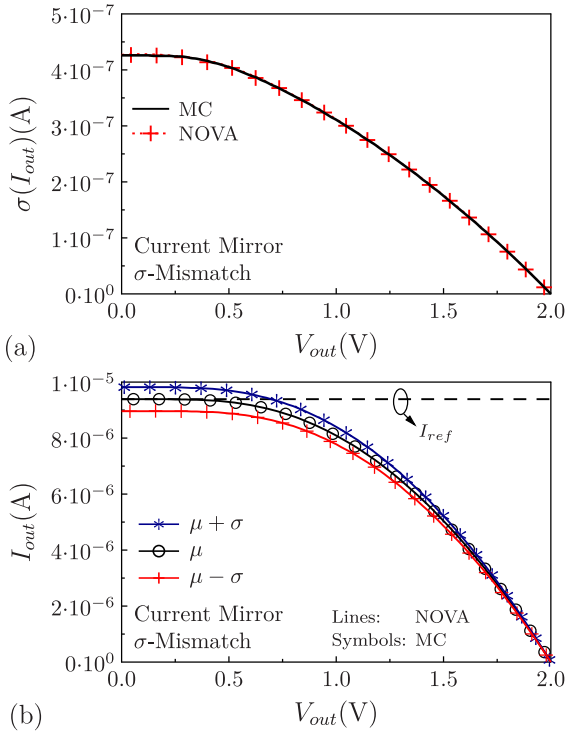

FIGURE 10. **(a) Standard deviation of the output current $\sigma(I_{out})$ of the current mirror of Fig. 9 as a function of the output voltage V_{out}. (b) Mean-value μ and corner-value $\mu \pm \sigma$ output currents of the same circuit. Symbols: Monte Carlo simulation with 5000 iterations. Solid lines: NOVA method. Dashed lines: Reference current I_{ref} of the mean-value μ model card.**

TABLE 3. **Simulation processing times.**

	5000-iteration MC	NOVA method
Source Follower	$\simeq$ 201 min	$\simeq$ 2 min
Inverter mismatch analysis	$\simeq$ 214 min	$\simeq$ 2 min
Inverter process variations	$\simeq$ 202 min	$\simeq$ 2 min
Current Mirror	$\simeq$ 210 min	$\simeq$ 2 min

The processing times required for the Monte Carlo method and the proposed NOVA method are listed in Table 3. NOVA offers an improvement of almost 99 % compared to the typical Monte Carlo simulation.

VII. CONCLUSION

An efficient alternative to the Monte Carlo statistical-analysis methodology that can be used for the variability study of integrated circuits has been presented. The proposed "Noise-Based Variability Approach" (NOVA) method has been tested on circuits based on organic TFTs and has been shown to be suitable for fast process and mismatch statistical circuit analyses. NOVA can be easily implemented through a small number of minor modifications to the Verilog-A transistor instances and by a few simple rearrangements of the circuit topology. Unlike Monte Carlo, the NOVA method is applicable only for Gaussian-shaped statistical distributions. The principle advantage of NOVA over Monte Carlo is the significantly shorter processing time, which makes NOVA beneficial for circuit designers.

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