Compact Modeling of Nonlinear Contact Effects in Short-Channel Coplanar and Staggered Organic Thin-Film Transistors

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***Abstract*— We present analytical physics-based compact models for the Schottky barriers at the interfaces between the organic semiconductor and the source and drain contacts in organic thin-film transistors (TFTs) fabricated in the coplanar and the staggered device architecture, and we illustrate the effect of these Schottky barriers on the current–voltage characteristics of the TFTs. The model for the source barrier explicitly considers the field-dependent barrier lowering due to image charges. Potential solutions have been derived by applying the Schwarz–Christoffel transformation, leading to expressions for the electric field at the source barrier and for the contact resistance at the source contact. With regard to the drain barrier, a generic compact-modeling scheme based on the current–voltage characteristics of a barrier-less TFT is introduced that can be applied to any compact dc model. Finally, both models are incorporated into an existing charge-based compact dc model and verified against the results of measurements performed on coplanar and staggered organic TFTs with channel lengths ranging from 0.5 to 10.5 μm.**

***Index Terms*— Compact modeling, contact effects, contact resistance, organic thin-film transistor (TFT), Schottky barrier, short channel.**

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I. Introduction

ORGANIC thin-film transistors (TFTs) can be fabricated at relatively low process temperatures and thus not only on glass but also on polymeric substrates [1], which makes them potentially useful for flexible active-matrix displays and sensor arrays [2], [3]. The design of such systems benefits greatly from efficient circuit simulations, which requires compact models that accurately reproduce the electrical TFT characteristics by capturing the relevant device physics. The electrical TFT characteristics are determined in large part by the properties of the organic semiconductor (e.g., orbital energies, charge-carrier mobility, and charge-trap density), the thickness of the organic semiconductor film [4] and the gate dielectric [5], the channel length, and various operational parameters, such as the applied gate–source and drain–source voltages and the temperature. Another important aspect is the device architecture, i.e., whether the TFTs are fabricated in the coplanar or the staggered device structure [5] (see Fig. 1).

While the channel resistance of organic TFTs is determined mainly by the channel length and the intrinsic channel mobility, the contact resistance is usually determined by the height of the Schottky barrier at the interface between the organic semiconductor and the source/drain contacts [6]. The height of this barrier is determined by the difference between the work function of the source/drain metal and the energy of the transport level of the organic semiconductor (i.e., the highest occupied molecular orbital (HOMO) for p-channel TFTs and the lowest unoccupied molecular orbital (LUMO) for n-channel TFTs). The barrier height and the contact resistance affect several TFT parameters, including the ON/OFF current ratio [7] and the severity of various short-channel effects, such as the nonlinearity in the output characteristics at small drain–source voltages [8]. The nonohmic charge injection across the metal–semiconductor interfaces in organic TFTs has been investigated in [9]. Note that previous approaches to model the contact properties of organic TFTs have been entirely [10], [11] or partially empirical [12] and have either considered only the Schottky barrier at the source but not the drain [11] or have neglected the barrier-lowering effect [12].

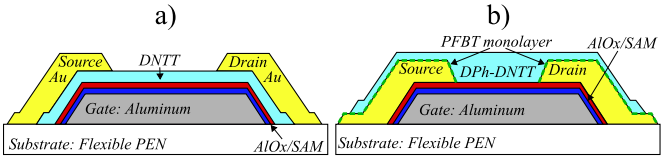


Fig. 1. Schematic cross section of organic TFTs fabricated in (a) staggered and (b) coplanar device architecture.

In addition, no existing contact model for organic TFTs has ever been incorporated into a compact current model in order to obtain a closed-form equation.

In this article, analytical physics-based compact models are derived for the bias-dependent Schottky barriers at the interfaces between the organic semiconductor and the source and drain contacts in coplanar and staggered organic TFTs (see Sections III and IV). These models are then incorporated into a recently presented charge-based compact current model [13]–[15] (summarized in Section II). Subsequently, the validity of the enhanced current model and its scalability with respect to the channel length are demonstrated by fitting the model to the measured current–voltage characteristics of coplanar and staggered organic TFTs with channel lengths ranging from 0.5 to 10.5 μm (see Section IV). In the following, the model equations will be derived for n-channel TFTs, but they can be easily adapted to p-channel TFTs. All energy diagrams and current–voltage characteristics will be shown for p-channel TFTs.

II. Charge-Based Modeling Approach

In [13], the following expression for the accumulated charge density close to the source/drain contacts based on a Gaussian distribution of the density of states (DOS) has been derived by solving Poisson's equation and using the first branch of Lambert's W function L_W:

$$Q'_{\mathrm{ms}/d} = \frac{\alpha kT}{q} C'_{\mathrm{diel}} \cdot L_W \left\{ \frac{q^2 d_m N_{\mathrm{st}}}{C'_{\mathrm{diel}} \alpha kT} \times \exp \times \left(\frac{V_{\mathrm{gs}/d} - V_{\mathrm{fb}} - E_g/2q - q N'_{t,\max}/C'_{\mathrm{diel}}}{\alpha kT/q} \right) \right\} \quad (1)$$

with Boltzmann's constant k, the temperature T, the elementary charge q, the unit-area gate-dielectric capacitance C'_{diel}, the thickness of the accumulated charge-carrier channel d_m, the density of shallow traps N_{st}, the maximum density of filled deep traps and interface states at threshold $N'_{t,\max}$, and the flat-band voltage V_{fb}. The parameter α describes the degradation of the subthreshold swing S with respect to the ideal thermal swing

$$\alpha = 1 + \frac{q^2 N'_t}{C'_{\mathrm{diel}}} = \frac{S}{\ln(10) kT/q}. \quad (2)$$

In the final equation for the drain current I_d, the carrier transport is described as drift-diffusion transport of quasi-free charge carriers, with the hopping-transport mechanism being accounted for by an effective charge-carrier mobility μ_{eff}

$$I_d = \mu_{\mathrm{eff}} W_{\mathrm{ch}} \left(\frac{kT}{q} \cdot \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md}}}{L_{\mathrm{ch}}} + \frac{Q'^2_{\mathrm{ms}} - Q'^2_{\mathrm{md}}}{2 L_{\mathrm{ch}} C'_{\mathrm{diel}}} \right) \times (1 + \lambda (V_{\mathrm{ds}} - V_{\mathrm{ds}x})) + V_{\mathrm{ds}}/R_{\mathrm{leak}} \quad (3)$$

$$\mu_{\mathrm{eff}} = \frac{\kappa \cdot \left(Q'_{\mathrm{ms}}/C'_{\mathrm{diel}} \right)^{\beta}}{1 + \kappa \cdot \left(Q'_{\mathrm{ms}}/C'_{\mathrm{diel}} \right)^{\beta} W_{\mathrm{ch}} R_c Q'_{\mathrm{ms}}/L_{\mathrm{ch}}}. \quad (4)$$

The model uses an empirical power-law mobility model [16] with parameters κ and β, incorporating a constant contact resistance R_c by a first-order approximation, similar to [17]. The exponent β affects the subthreshold swing calculated by the compact model, which means that the subthreshold-swing parameter S in (2) will generally be different from the subthreshold swing S_{obs} observed in the measured current–voltage characteristics. The relationship between the subthreshold swing calculated by the compact model (S) and the subthreshold swing observed in the measured current–voltage characteristics (S_{obs}) can be written as

$$S = (1 + \beta) S_{\mathrm{obs}}. \quad (5)$$

For the staggered TFT architecture, the field-independent contact resistance R_c can be calculated according to [18] by considering the contact length L_c and an additional contribution of an extended contact length L_{ext}

$$R_c = 2 R_{\mathrm{sheet}} L_T \cdot \coth((L_c + L_{\mathrm{ext}})/L_T)/W_{\mathrm{ch}} \quad (6)$$

with the sheet resistance of the semiconductor layer R_{sheet} [18] and the characteristic length L_T [19] that is defined as the contact length over which 63% of the charge-carrier injection between the metal and the semiconductor occurs. The effect of channel-length modulation is accounted for by the parameter λ in 3) and by the following expression:

$$V_{\mathrm{ds}x} = \left(Q'_{\mathrm{ms}} - Q'_{\mathrm{md}} \right)/C'_{\mathrm{diel}}. \quad (7)$$

It was shown in [13] that the charge densities at the source and drain ends of the channel can be calculated from the values of the threshold voltage V_T and the subthreshold swing, which greatly simplifies the procedure of fitting the compact model to the measurement data

$$Q'_{\mathrm{ms}/d} = \frac{\alpha kT}{q} C'_{\mathrm{diel}} \cdot L_W \left\{ \exp\left(\frac{V_{\mathrm{gs}/d} - V_T}{\alpha kT/q} \right) \right\}. \quad (8)$$

Together with (2) and (3), a compact and one-piece expression for the drain current is obtained, which relates to the threshold voltage and the subthreshold swing. Short-channel effects in staggered TFTs are captured by the model as subthreshold-swing degradation, threshold-voltage roll-off and drain-induced barrier lowering (DIBL), as detailed in [15].

One aspect that is not explicitly included in this model is the trap-induced hysteresis in the current–voltage characteristics, so this important feature is accounted for by the following empirical approach [15]:

$$\Delta V_{\mathrm{hys}} = V_{\mathrm{ds}} \cdot f_{\mathrm{hys}} \quad (9)$$

where f_{hys} is a parameter determined by the sweep rate during the measurement of the transfer characteristics. Finally, ΔV_{hys} is implemented into the threshold voltage V_T of the current compact model.

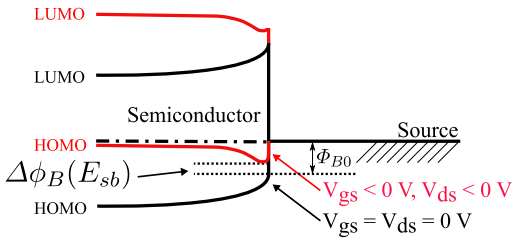


Fig. 2. Energy diagrams of the interface between the organic semiconductor and the source contact of a p-channel organic TFT. Application of negative gate–source and drain–source voltages causes the barrier height to decrease by $\Delta\Phi_B$ (shown in red).

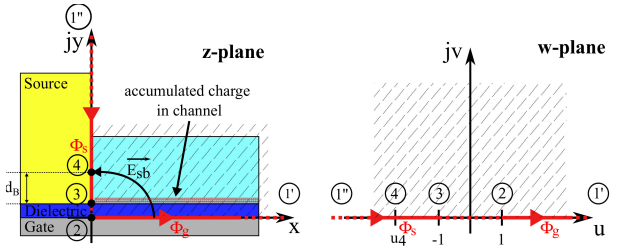


Fig. 3. Conformal mapping technique applied at the source end of a coplanar TFT.

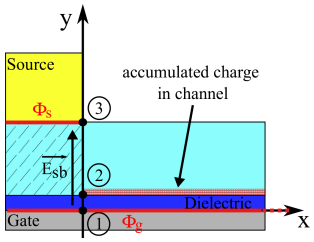


Fig. 4. Schematic cross section of the source-sided half of a staggered organic TFT.

III. Modeling of the Schottky Barrier at the Source Contact

The source/drain contacts of organic TFTs are usually metallic, which means that a Schottky barrier typically exists at the interface between the contacts and the organic semiconductor. The efficiency of charge-carrier injection over this Schottky barrier is controlled by the barrier height, which in turn is determined by the difference between the metal work function Φ_m and the energy of the transport level in the semiconductor (i.e., HOMO for p-channel TFTs and LUMO for n-channel TFTs) [20], [21]

$$\text{n-channel TFT: } \Phi_{B0} = \Phi_m - \text{LUMO} \tag{10}$$

$$\text{p-channel TFT: } \Phi_{B0} = \Phi_m - \text{HOMO}. \tag{11}$$

However, the effective Schottky barrier height Φ_B is slightly smaller than Φ_{B0} since the potential profile is sensitive to the electric field at the barrier. A charge carrier located in the semiconductor at a distance x from the interface induces an "image charge" on the metal surface. The resulting force of attraction between the charge carrier and the metal is equivalent to a force between an electron and an equal (but positive) charge separated by a distance of $2\times$ and produces a barrier lowering of [20]

$$\Delta\phi_B = \sqrt{q E_{\text{sb}}/(4\pi\varepsilon_{\text{sc}})} \tag{12}$$

with the electric field at the barrier E_{sb} and the permittivity of the semiconductor ε_{sc}. Fig. 2 shows schematically the energy diagram of the metal–semiconductor interface of an organic TFT with and without application of gate–source and drain–source voltages, illustrating the barrier-lowering effect. The nonlinearity in the output characteristics at small drain–source voltages can be attributed to the relatively large barrier height at low voltages and the reduction of this barrier height with increasing gate–source and drain–source voltages.

A. Decomposition of Poisson's Equation

To derive an analytical closed-form expression for the electric field E_{sb} for calculating the barrier lowering according to (12), Poisson's equation must be solved. A decomposition strategy is thus applied [22], which leads to a simplified version of Poisson's equation with a 2-D solution φ of the Laplacian differential equation and a 1-D particular solution Φ_p describing the space charges within the accumulation channel

$$\Delta\Phi(x,y) = -\frac{\rho}{\varepsilon} = \Delta\varphi(x,y) + \frac{d\Phi_p(y)}{dy} \tag{13}$$

with

$$\Delta\varphi(x,y) = 0 \quad \text{and} \quad \frac{d\Phi_p(y)}{dy} = -\frac{\rho(y)}{\varepsilon} \tag{14}$$

where $\rho(y)$ is the space-charge profile in the direction perpendicular to the plane of the gate electrode and ε is the permittivity within the region of interest. If the drain current is limited by the source barrier, most of the drain–source voltage V_{ds} will drop across this barrier, and the voltage drop along the channel will be negligible. Thus, the charge density at the drain end of the channel and within the channel up to the source barrier can be equated and calculated using Q'_{md} [see (1)]. Also, assuming that the gate-induced carrier channel has a thickness of no more than a few molecular monolayers [23], the charge distribution in the carrier channel can be approximated as a charge layer at the gate-dielectric/semiconductor interface. Thus, the following 1-D particular solution $\Phi_p(y)$ can be defined for the coordinate system shown in Fig. 3 for coplanar TFTs and in Fig. 4 for staggered TFTs:

$$\Phi_p(y) = \begin{cases} Q'_{\text{md}}/C'_{\text{diel}}, & \text{for } y = 0 \\ Q'_{\text{md}}/\varepsilon_{\text{diel}} \cdot (t_{\text{diel}} - y), & \text{for } 0 < y < t_{\text{diel}} \\ 0, & \text{for } y \geq t_{\text{diel}} \end{cases} \tag{15}$$

where t_{diel} is the gate-dielectric thickness and $\varepsilon_{\text{diel}}$ is the permittivity of the gate dielectric. In order to fulfill the criteria for the decomposition strategy, the boundary conditions for the solution φ of the Laplace differential equation must be transformed [22]

$$\varphi(x,y) = \Phi(x,y) - \Phi_p(y). \tag{16}$$

B. Boundary Conditions

The boundary conditions for the source and gate electrodes incorporating the 1-D solution of the decomposition strategy

[see (16)] are defined as

$$\Phi_s = V_s - V_{\text{bi}} \tag{17}$$
$$\Phi_g = V_g - V_{\text{fb}} - Q'_{\text{md}}/C'_{\text{diel}}. \tag{18}$$

The corresponding built-in voltage V_{bi} and the flat-band voltage V_{fb} are defined as follows:

$$V_{\text{bi}} = \Phi_{m,s} - (\text{LUMO} + E_g/(2q)) \tag{19}$$
$$V_{\text{fb}} = \Phi_{m,g} - (\text{LUMO} + E_g/(2q)) \tag{20}$$

where $\Phi_{m,g}$ is the work function of the gate metal, $\Phi_{m,s}$ is the work function of the source metal, and E_g is the difference between the LUMO and HOMO energies of the semiconductor. The voltage drop $Q'_{\text{md}}/C'_{\text{diel}}$ follows from the decomposition strategy outlined in Section III-A. In the calculation of the potential problem, this voltage drop can be considered as the effect of a charge layer partially shielding the source barrier from the gate field.

The potential difference $\Phi_g - \Phi_s$ required to calculate the electric field can be simplified using (10), (11), and (17)–(19) to

$$\Phi_g - \Phi_s = V_{\text{gs}} - V_{T,\text{ideal}} - Q'_{\text{md}}/C'_{\text{diel}} + \Phi_{B0} \tag{21}$$

where $V_{T,\text{ideal}}$ can be treated as an initial threshold-voltage condition for a trap-less organic TFT with an intrinsic semiconductor

$$V_{T,\text{ideal}} = V_{\text{fb}} \pm E_g/2q. \tag{22}$$

The sign is positive for n-channel TFTs and negative for p-channel TFTs. To capture shallow traps and deep traps, $V_{T,\text{ideal}}$ is replaced by the threshold voltage V_T of the charge-based current model [see (8)], and subsequently, $V_{\text{gs}} - V_T$ is replaced by $Q'_{\text{ms}}/C'_{\text{diel}}$

$$\Phi_g - \Phi_s = \left(Q'_{\text{ms}} - Q'_{\text{md}}\right)/C'_{\text{diel}} + \Phi_{B0}. \tag{23}$$

C. Electric Field in Coplanar TFTs

In order to solve the homogeneous Laplace differential equation $\Delta\varphi = 0$ for the coplanar device architecture, the conformal mapping technique, Schwarz–Christoffel transformation, is applied. To do this, an analytical mapping function $w = f(z)$ is derived that maps a complex geometry from the plane $z = x + jy$ to a simpler geometry in the plane $w = u + jv$ (see Fig. 3). The region of interest in the z plane is transformed onto the upper half of the w plane (hatched area in Fig. 3). The corresponding boundaries in the z plane are now located on the horizontal axis of the coordinate system in the w plane. To obtain a homogeneous domain in the region of interest and to fulfill the conditions of a Laplace differential equation, the gate-dielectric thickness t_{diel} is scaled

$$\tilde{t}_{\text{diel}} = t_{\text{diel}} \cdot \varepsilon_{\text{sc}}/\varepsilon_{\text{diel}}. \tag{24}$$

This approximation is valid as long as the channel length is much greater than the gate-dielectric thickness [22]. According to the Schwarz–Christoffel transformation, the geometries in the z plane and the w plane of Fig. 3 are related to each other by the following derivative [24]:

$$\frac{\mathrm{d}z}{\mathrm{d}w} = C_1 \cdot \frac{1}{\sqrt{w-1}} \tag{25}$$

with the constant C_1. Integrating over w leads to the indefinite mapping function

$$z = f(w) = 2C_1\sqrt{w-1} + C_2. \tag{26}$$

The unknown constants C_1 and C_2 are determined from the TFT geometry [24]

$$C_1 = \tilde{t}_{\text{diel}}/(2\sqrt{2}) \quad \text{and} \quad C_2 = 0 \tag{27}$$

and lead finally to the following mapping function $z = f(w)$ and its inverse function $w = f^{-1}(z)$:

$$z = \sqrt{w-1} \cdot \tilde{t}_{\text{diel}}/\sqrt{2} \tag{28}$$
$$w = 1 + 2 \cdot z^2/\tilde{t}^2_{\text{diel}}. \tag{29}$$

An analytical solution for the potential problem of the geometry shown in Fig. 3 (two electrodes separated by a gap) was presented in [24]:

$$P_w = \Phi_g + j(\Phi_g - \Phi_s)\cosh^{-1}(w)/\pi. \tag{30}$$

The corresponding electric field in the w plane is obtained by differentiation [24]

$$E_w = -\frac{dP_w}{dw} = -j\frac{\Phi_g - \Phi_s}{\pi\sqrt{w-1}\sqrt{w+1}}. \tag{31}$$

In order to obtain the absolute electric field in the z plane, $|E_w|$ can be transformed using the absolute reciprocal mapping derivative

$$|E_z| = |E_w|\left|\frac{dw}{dz}\right| = \left|-j\frac{2\sqrt{2}}{\tilde{t}_{\text{diel}}} \cdot \frac{\Phi_g - \Phi_s}{\pi\sqrt{w+1}}\right|. \tag{32}$$

Equations (29) and (32) with the boundary conditions (17) and (18) make it possible to calculate the absolute electric field for a specific point $z = x + jy$ in the z plane. However, the current is injected over an extended area across the source/semiconductor interface, and the current density is not constant across this area. We thus introduce a fitting parameter of a representative barrier position d_B for the entire injection area, which defines the distance between points 3 and 4 in Fig. 3. The representative injection point $z_4 = j(\tilde{t}_{\text{diel}} + d_B)$ inserted into the inverse mapping function (29) yields

$$w_4 = 1 - 2 \cdot (\tilde{t}_{\text{diel}} + d_B)^2/\tilde{t}^2_{\text{diel}}. \tag{33}$$

Finally, (32) can be simplified for point 4 that models the electric field at the Schottky barrier of the source contact

$$E_{\text{sb,copl}} = \frac{2}{\pi} \cdot \frac{\Phi_g - \Phi_s}{\sqrt{2d_B\tilde{t}_{\text{diel}} + d_B^2}}. \tag{34}$$

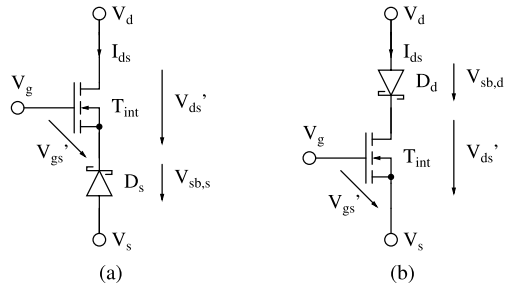


Fig. 5. Equivalent circuits of an n-channel organic TFT in which the drain current is limited by the Schottky barrier at (a) source or (b) drain contact.

D. Electric Field in Staggered TFTs

Fig. 4 shows a schematic cross section of the source-sided half of a staggered organic TFT. The charge-carrier injection occurs across the source/semiconductor interface within the gate-to-source overlap region (hatched area). Most of the charges are injected within a short distance from the coordinate origin [19]. In the overlap region, the solution to the Laplacian differential equation depends essentially only on coordinate y, so a 1-D analysis is sufficient to derive the following equation for the electric field at the Schottky barrier:

$$E_{\mathrm{sb,stag}} = \frac{\Phi_g - \Phi_s}{t_{\mathrm{sc}} + \tilde{t}_{\mathrm{diel}}} \tag{35}$$

where t_{sc} is the thickness of the semiconductor.

E. Model Implementation

The Schottky barrier at the source/semiconductor interface is modeled as a reverse-biased diode D_s [see Fig. 5(a)] connected in series with the intrinsic transistor T_{int}. The current–voltage characteristics of the source barrier are modeled using the diode equation [20]

$$I_{D,s} = -I_{s,s} \cdot (\exp(-q V_{\mathrm{sb},s}/(\theta k T)) - 1) \tag{36}$$

with the voltage drop across the barrier $V_{\mathrm{sb},s}$, the nonideality factor of the diode θ, and the reverse-bias saturation current $I_{s,s}$. Charge-carrier injection across a metal–semiconductor interface typically occurs by thermionic emission over the barrier or by quantum-mechanical tunneling through the barrier. In the case of intrinsic organic semiconductors, the small charge density leads to a relatively large depletion width [6], so the tunneling current can be ignored and the injection current can be described based solely on the thermionic-emission theory

$$I_{s,s} = W_{\mathrm{ch}} L_{\mathrm{inj}} A^* T^2 \exp(-q(\Phi_{B0} - \Delta\Phi_B)/(\eta k T)) \tag{37}$$

where T is the temperature, η is the nonideality factor of the reverse-bias saturation current, and the effective Richardson constant $A^* = 120\,\mathrm{A/(cm^2\,K^2)}$. In staggered TFTs, the injection length L_{inj} is identical to the characteristic length L_T as defined for (6) [19]. For coplanar TFTs, L_{inj} is assumed to be identical to the thickness of the charge-carrier channel.

In the linear regime of operation, the height of the Schottky barrier at the source contact of an organic TFT can be quite large, in which case the drain current may be limited by the contact resistance, rather than the channel resistance. The voltage drop along the channel will then be negligible, and the drain–source voltage V_{ds} will drop almost entirely across the Schottky barrier. In the saturation regime, the voltage drop across the Schottky barrier saturates at a value equal to the drain–source saturation voltage ($V_{\mathrm{ds}} = V_{\mathrm{gs}} - V_T$). Equation (7) of the charge-based current model provides a one-piece expression that covers the linear and the saturation regime

$$V_{\mathrm{sb},s} \approx V_{\mathrm{ds}x} = \left(Q'_{\mathrm{ms}} - Q'_{\mathrm{md}}\right)/C'_{\mathrm{diel}}. \tag{38}$$

The expressions for the voltage drop across the barrier $V_{\mathrm{sb},s}$ and the current over the barrier $I_{D,s}$ make it possible to define an equivalent and nonlinear Schottky-barrier resistance at the source contact

$$R_{\mathrm{sb},s} = V_{\mathrm{sb},s}/(-I_{s,s} \cdot (\exp(-q V_{\mathrm{sb},s}/(\theta k T)) - 1)). \tag{39}$$

Since $R_{\mathrm{sb},s}$ is connected in series with the field-independent resistance R_c in (4), R_c can be replaced with

$$R_{c,\mathrm{total}} = R_c + R_{\mathrm{sb},s}. \tag{40}$$

IV. Modeling of the Schottky Barrier at the Drain Contact

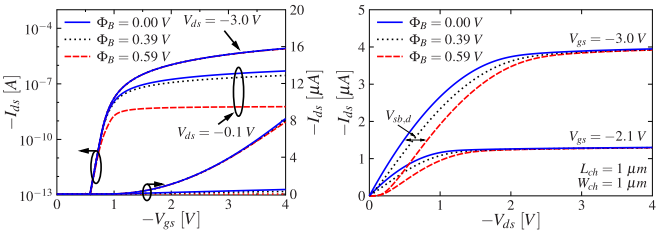
In contrast to the barrier at the source contact, the Schottky barrier at the drain contact is operated in the forward direction. The diode-current equation based on the equivalent circuit in Fig. 5(b) is defined as

$$I_{D,d} = I_{s,d} \cdot (\exp(q V_{\mathrm{sb},d}/(\theta k T)) - 1) \tag{41}$$

with the reverse-bias saturation current $I_{s,d}$

$$I_{s,d} = W_{\mathrm{ch}} L_{\mathrm{inj}} A^* T^2 \exp(-q\Phi_{B0}/(\eta k T)). \tag{42}$$

According to Fig. 5(b), the drain barrier does not affect the gate–source voltage V_{gs}, but it does cause a reduction of the drain–source voltage of the intrinsic transistor V'_{ds}. When the voltage drop across a generic forward-biased diode is smaller than the forward voltage V_F, the diode current is very small, while for voltages beyond V_F, the exponential relationship between current and voltage causes the voltage drop to essentially saturate near V_F, and the diode current can be very large. Applying these general considerations to the Schottky barrier at the drain contact of an organic TFT, we can distinguish the two regimes $V_{\mathrm{ds}} < V_F$ and $V_{\mathrm{ds}} > V_F$. When $V_{\mathrm{ds}} < V_F$, the barrier is limiting the drain current of the TFT, whereas when $V_{\mathrm{ds}} > V_F$, the voltage drop across the barrier $V_{\mathrm{sb},d}$ saturates and is independent of V_{ds}. Fig. 6 shows the results of TCAD simulations to illustrate the effect of the drain barrier on the output and transfer characteristics of a staggered organic TFT. In the transfer characteristics, it can be seen that the threshold voltage and the subthreshold swing are independent of the barrier height, i.e., the subthreshold regime is not affected by the drain barrier. The saturation regime is also not affected by the drain barrier, as both the transfer characteristics and the output characteristics indicate that the drain current at large negative drain–source voltages is independent of the drain-barrier height, since $V_{\mathrm{ds}} > V_F$ and



(a) (b)

Fig. 6. Results of TCAD simulations illustrating the effect of the drain barrier on the transfer and output characteristics of a staggered p-channel TFT with a channel length and width of 1 μm for three different drain-barrier heights. (a) Transfer characteristics. (b) Output characteristics.

thus $V_{\mathrm{sb},d} = \text{const}$. Thus, $V_{\mathrm{sb},d}$ can be calculated from the drain current of a barrier-less transistor $I_{\mathrm{ds,bl}}$ in the saturation regime by equating $I_{\mathrm{ds,bl}}$ and $I_{D,d}$ of (41). In this work, we calculate $I_{\mathrm{ds,bl}}$ at the operation point $V_{\mathrm{ds}} = 5 \cdot (V_{\mathrm{gs}} - V_T)$ using the current model in (3), but any other suitable model can also be applied. Rearranging $I_{\mathrm{ds,bl}} = I_{D,d}$ with (41) and (42) leads to the voltage drop across the drain barrier in the saturation regime

$$V_{\mathrm{sb},d,\mathrm{sat}} = \theta kT/q \cdot \ln(I_{d,\mathrm{bl}}/I_{\mathrm{sb},d} + 1). \tag{43}$$

If $V_{\mathrm{ds}} = 0$, then $V_{\mathrm{sb},d} = 0$ and $I_{\mathrm{ds}} = 0$. In order to cover all meaningful positive values of V_{ds}, the voltage drop across the barrier $V_{\mathrm{sb},d}$ is modeled as a linear function of V_{ds} between $V_{\mathrm{ds}} = 0$ and the operation point at which $V_{\mathrm{sb},d}$ saturates. The results of the TCAD simulations in Fig. 6(b) indicate that the drain–source voltage at which the voltage drop across the drain barrier saturates is larger than the drain–source voltage at which the drain current saturates. In other words, there exists a range of drain–source voltages at which the drain current is already in saturation, but the voltage drop across the drain barrier is not. Therefore, the condition for $V_{\mathrm{sb},d}$ to saturate is defined with the help of an additional fitting parameter w_{sat}

$$V_{\mathrm{ds},V_{\mathrm{sbd-sat}}} = w_{\mathrm{sat}} \cdot (V_{\mathrm{gs}} - V_T). \tag{44}$$

The expression $V_{\mathrm{gs}} - V_T$ is replaced by $Q'_{\mathrm{ms}}/C'_{\mathrm{diel}}$. Subsequently, $V_{\mathrm{sb},d}$ can be defined as

$$V_{\mathrm{sb},d} = \begin{cases} V_{\mathrm{ds}} \dfrac{V_{\mathrm{sb},d,\mathrm{sat}} C'_{\mathrm{diel}}}{w_{\mathrm{sat}} Q'_{\mathrm{ms}}}, & \text{for } 0 \le V_{\mathrm{ds}} < \dfrac{w_{\mathrm{sat}} Q'_{\mathrm{ms}}}{C'_{\mathrm{diel}}} \\ V_{\mathrm{sb},d,\mathrm{sat}}, & \text{for } V_{\mathrm{ds}} > \dfrac{w_{\mathrm{sat}} Q'_{\mathrm{ms}}}{C'_{\mathrm{diel}}}. \end{cases} \tag{45}$$

A smoothing function as in [25] prevents the numerical problems and discontinuities in the current–voltage characteristics

$$\begin{aligned} V_{\mathrm{sb},d} &= C(1 - 1/B \cdot \ln(1 + \exp(A(1 - x/C)))) \\ x &= V_{\mathrm{ds}} \cdot V_{\mathrm{sb},d,\mathrm{sat}} C'_{\mathrm{diel}} \big/ \left(w_{\mathrm{sat}} \cdot Q'_{\mathrm{ms}}\right), \quad A = 5 \\ B &= \ln(1 + \exp(A)), \quad C = V_{\mathrm{sb},d,\mathrm{sat}}. \end{aligned} \tag{46}$$

Finally, the drain–source voltage V_{ds} of the current model in (1) or (8) is replaced by the following expression to enhance the charge-based dc model with the impact of the Schottky barrier at the drain contact:

$$V_{\mathrm{ds,new}} = V_{\mathrm{ds}} - V_{\mathrm{sb},d}. \tag{47}$$

TABLE I
CHANNEL-WIDTH-NORMALIZED CONTACT RESISTANCE OF THE COPLANAR DPH-DNTT TFTS FOR EACH CHANNEL LENGTH FOR WHICH THE COMPACT CURRENT MODEL PROVIDED THE BEST FIT TO THE MEASUREMENT RESULTS (SEE FIG. 7)

L_{ch} $[\mu m]$	10.5	4.5	2.4	1.4	1.0
$R_c W_{ch}$ $[\Omega cm]$	77.5	41	25	15.75	12.1

V. RESULTS AND VERIFICATION

In this section, the compact models derived for the Schottky barriers at the source and drain contacts are verified and discussed based on measured current–voltage characteristics of coplanar and staggered organic TFTs. Both compact models are implemented into the current model summarized in Section II and then fitted to the measurement data.

The TFTs were fabricated on flexible polyethylene naphthalate (PEN) substrates. The gate electrodes (aluminum), the source and drain contacts (gold), and the organic semiconductors were deposited by thermal evaporation or sublimation in vacuum and patterned using high-resolution silicon stencil masks [8], [26], [27]. The gate dielectric is a stack of oxygen-plasma-grown aluminum oxide and an n-tetradecylphosphonic acid self-assembled monolayer with a total thickness (t_{diel}) of approximately 8 nm [28]. The small-molecule semiconductors 2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DPh-DNTT) [27] and dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [8] were used for the coplanar and staggered TFTs, respectively, with a nominal thickness (t_{sc}) of 25 nm. The source and drain contacts have a thickness (t_{co}) of 30 nm. For the coplanar TFTs, the surface of the source and drain contacts was modified with a monolayer of pentafluorobenzenethiol (PFBT) prior to the DPh-DNTT deposition [5]. The coplanar TFTs have channel lengths (L_{ch}) ranging from 1 to 10.5 μm and a channel width (W_{ch}) of 50 μm. The staggered TFTs have channel lengths ranging from 0.5 to 1 μm and a length/width ratio of 15.

To demonstrate the excellent scalability of the compact models, the goal of the fitting procedure was to maximize the number of parameters whose values can be chosen independently of the channel length. Fig. 7 shows the results from the compact model fitted to results from measurements performed on coplanar DPh-DNTT TFTs with channel lengths of 1, 2.4, and 10.5 μm [27]. Since all transistors have the same channel width, a much larger drain current is observed for smaller channel lengths. Furthermore, the superlinear relation between drain current and drain–source voltage in the linear regime of the output characteristics is more pronounced for smaller channel lengths, confirming that reducing the channel length causes the drain current to be increasingly limited by the Schottky barriers at the source and drain contacts, rather than by the channel resistance. The transfer characteristics indicate a weak dependence of the threshold voltage on the drain–source voltage that is possibly due to charge traps. Table I shows that the model indicates a significant and monotonic dependence of the contact resistance on the channel length. The reason for this is unknown. To first order, the contact resistance should be independent of the channel length (which is, among other things, a fundamental assumption for the transmission line

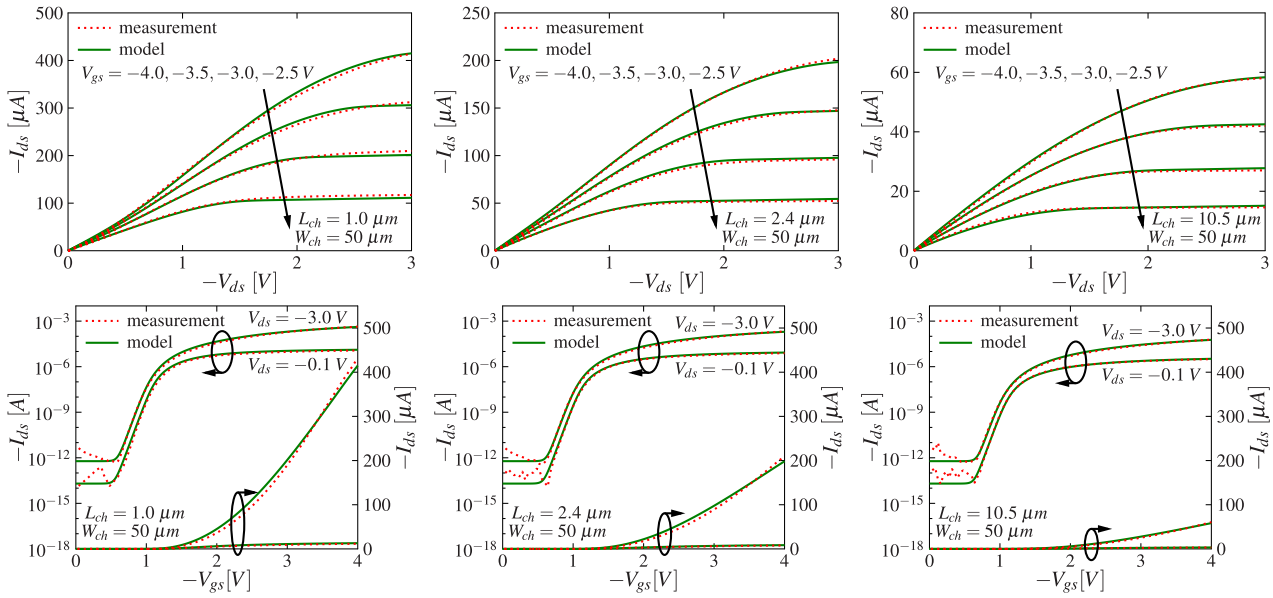


Fig. 7. Output and transfer characteristics of coplanar DPh-DNTT TFTs with channel lengths of 1, 2.4, and 10.5 μm calculated using the compact model (green lines) and, for comparison, obtained from measurements.

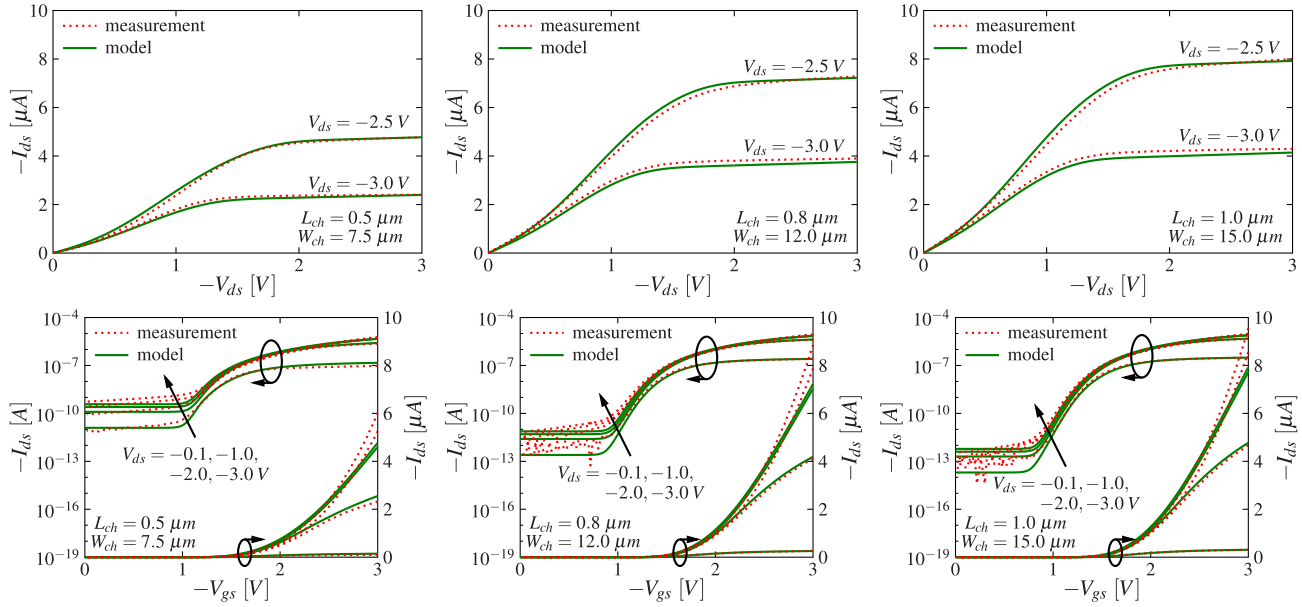


Fig. 8. Output and transfer characteristics of staggered DNTT TFTs with channel lengths of 0.5, 0.8, and 1 μm calculated using the compact model (green lines) and, for comparison, obtained from measurements.

method). A previous modeling study also reported a (slight) dependence of the contact resistance of organic TFTs on the channel length [9], albeit for staggered, rather than coplanar TFTs. The large dependence of the width-normalized contact resistance on the channel length observed here may require further analysis that is beyond the scope of this study. The channel-length-independent parameters are: drain–source leakage resistance $R_{\text{leak}} = 5\,\text{T}\Omega$, parameter of the power-law mobility model $\kappa = 6.7\,\text{cm}^2/(\text{sV}^{\beta+1})$ and $\beta = 0.65$, threshold voltage $V_T = -1.06\,\text{V}$, observed subthreshold swing $S_{\text{obs}} = 80\,\text{mV/decade}$, injection length $L_{\text{inj}} = 2\,\text{nm}$, representative barrier position $d_B = 1.92\,\text{nm}$, initial barrier height $\Phi_{B0} = 0.455\,\text{eV}$, sweep-rate fitting parameter $f_{\text{hys}} = 0.025$, fitting parameter for the saturation voltage of the drain barrier $\omega_{\text{sat}} = 5$, and nonideality factors of the diode $\theta = 5$ and the diode's saturation current $\eta = 1.85$.

Fig. 8 shows the results of the compact model fitted to the results of measurements performed on staggered DNTT TFTs with channel lengths of 0.5, 0.8, and 1 μm [26]. The channel-length-independent parameters are: threshold voltage $V_T = -1.2\,\text{V}$, observed subthreshold swing $S_{\text{obs}} = 90\,\text{mV/decade}$, characteristic injection length $L_{\text{inj}} = 2.6\,\mu\text{m}$, sweep rate fitting parameter $f_{\text{hys}} = 0.02$, initial barrier height $\Phi_{B0} = 0.35\,\text{eV}$, and nonideality factors of the diode $\theta = 3.5$ and the diode's saturation current $\eta = 0.66$. Table II shows that the values of the parameters κ and β decrease with

TABLE II
TRANSISTOR PARAMETERS OF THE STAGGERED DNTT TFTS FOR EACH CHANNEL LENGTH FOR WHICH THE COMPACT CURRENT MODEL PROVIDED THE BEST FIT TO THE MEASUREMENT RESULTS (SEE FIG. 8)

L_{ch} $[\mu m]$	κ $[cm^2/V^{\beta+1}s^{-1}]$	β []	R_{leak} $[G\Omega]$	R_cW_{ch} $[\Omega cm]$	w_{sat} []
1.0	2.273	1.52	5000	117.15	11
0.8	2.214	1.57	400	102.82	9.5
0.6	1.672	1.42	10	85.28	4
0.5	0.864	1.00	8	83.20	3

decreasing channel length, which indicates an decreasing concentration of charge carriers in the channel based on the Gaussian DOS and the variable range hopping model [29]. The observed decrease of the leakage resistance R_{leak} with decreasing channel length reflects the expected increase in the OFF-state drain current upon reducing the source–drain distance. The parameter w_{sat} is greater than unity for all channel lengths, which confirms that the drain–source voltage at which the voltage drop across the drain barrier saturates is larger than the drain–source voltage at which the drain current saturates. However, the fact that the value of w_{sat} decreases with decreasing channel length indicates that the difference between the values of the drain–source voltage at which the voltage drop across the barrier and the drain current are saturating decreases with decreasing channel length.

VI. CONCLUSION

We have presented analytical closed-form physics-based compact models for the Schottky barriers at the interfaces between the organic semiconductor and the source and drain contacts in organic TFTs fabricated in the coplanar and the staggered device architecture. With regard to the source barrier, expressions for the contact resistance have been derived. The generic compact-modeling scheme for the drain barrier defines the voltage drop across the drain barrier on the basis of the saturation drain current of a barrier-less transistor. Both compact models have been incorporated into an existing charge-based dc model and verified against the results of measurements performed on coplanar and staggered organic TFTs. The enhanced current model shows excellent scalability for channel lengths as small as 0.5 μm.

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