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Flexible megahertz organic transistors and the critical role of the device geometry on their dynamic performance

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ABSTRACT

The development of organic thin-film transistors (TFTs) for high-frequency applications requires a detailed understanding of the intrinsic and extrinsic factors that influence their dynamic performance. This includes a wide range of properties, such as the device architecture, the contact resistance, parasitic capacitances, and intentional or unintentional asymmetries of the gate-to-contact overlaps. Here, we present a comprehensive analysis of the dynamic characteristics of the highest-performing flexible organic TFTs reported to date. For this purpose, we have developed the first compact model that provides a complete and accurate closed-form description of the frequency-dependent small-signal gain of organic field-effect transistors. The model properly accounts for all relevant secondary effects, such as the contact resistance, fringe capacitances, the subthreshold regime, charge traps, and non-quasistatic effects. We have analyzed the frequency behavior of low-voltage organic transistors fabricated in both coplanar and staggered device architectures on flexible plastic substrates. We show through S-parameter measurements that coplanar transistors yield more ideal small-signal characteristics with only a weak dependence on the overlap asymmetry. In contrast, the high-frequency behavior of staggered transistors suffers from a more pronounced dependence on the asymmetry. Using our advanced compact model, we elucidate the factors influencing the frequency-dependent small-signal gain and find that even though coplanar transistors have larger capacitances than staggered transistors, they benefit from substantially larger transconductances, which is the main reason for their superior dynamic performance.

I. INTRODUCTION

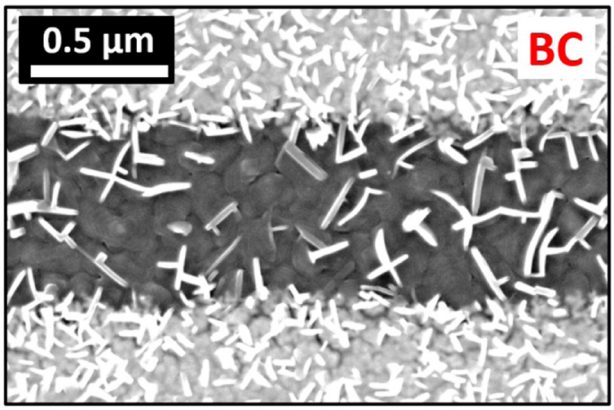
Thin-film transistors (TFTs) based on organic semiconductors (OSC) have been the subject of intense research for their possible use in novel electronics applications, ranging from wearable biometric sensors to active-matrix displays. The strong interest is primarily owing to the possibility of using room-temperature fabrication approaches to implement TFTs and circuits on flexible substrates, such as plastic foils and paper.[1–4] However, expansion of the possible application space for any TFT technology depends strongly on the ability of the TFTs to operate at suitably high frequencies without significant loss of signal amplification.[5] For example, active-matrix organic light-emitting diode (AMOLED) displays require the TFTs employed in the backplane to drive each pixel to be able to switch a signal at frequencies of up to several

tens of megahertz, depending on the display resolution and frame rate,[6] and the circuits in near-field radio frequency identification (RFID) tags need to be able to respond to input signals of 13.56 MHz.[7] Thus, a major portion of the research focus has been placed on increasing the maximum operational frequency of organic TFTs.[8] Recent advancements in device fabrication have led to the demonstration of high-frequency organic TFTs and circuits.[9–11] However, for the efficient design of reliable circuits, it is essential to consider the more-detailed frequency dependence of the signal-amplification capabilities of a given TFT technology. In this work, we present a deep analysis of the small-signal current gain ($h_{21} = i_d/i_g$) of organic thin-film transistors fabricated in the two different architectures that are most often used: the bottom-gate top-contact (TC) and the bottom-gate bottom-contact (BC) architectures. We describe the frequency-dependent small-signal gain using a customized compact model. We will first give some basic information about the general procedure of determining the small-signal gain and then analyze the points where problems occur when applying the theory to organic TFTs. Subsequently, we present our compact model and show the agreement with measured small-signal gains that is achievable.

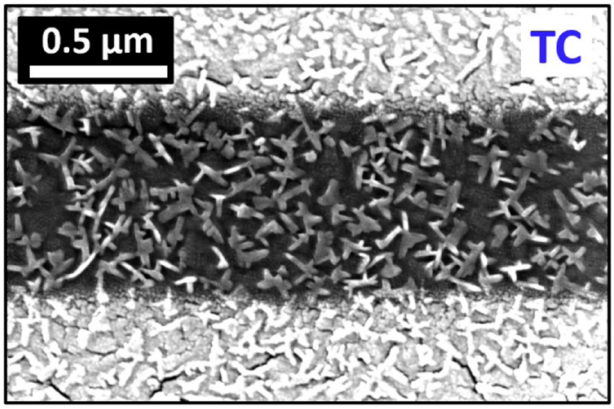
II. OTFT FABRICATION AND MEASUREMENTS

Bottom-gate bottom-contact (BC) and bottom-gate top-contact (TC) organic TFTs were fabricated on 125-μm-thick polyethylenenaphthalate (PEN) sheets (Teonex Q65 PEN; provided by W. A. MacDonald, DuPont Teijin Films, Wilton, United Kingdom) using high-resolution silicon stencil mask lithography.[12] Separate masks were used to pattern the interconnects, gate electrodes, source and drain contacts, and organic semiconductor layers. A hybrid gate dielectric with a total thickness of approximately 8 nm was prepared by exposing the aluminum gate electrodes to oxygen plasma (Oxford Instruments, 30 sccm oxygen, 10 mTorr, 200 W, 30 s) and subsequently immersing the substrate into a 1 mM 2-propanol solution of n-tetradecylphosphonic acid (TDPA; PCI Synthesis, Newburyport, MA, USA) to allow a self-assembled monolayer (SAM) to form on the aluminum oxide surface.[13] For BC TFTs, the gold source and drain contacts were then deposited by thermal evaporation in vacuum, and the substrates were subsequently immersed into a 10 mM solution of pentafluorobenzenethiol (PFBT; Santa Cruz Biotechnology, Heidelberg, Germany) in ethanol (nondenatured) for 30 min in a covered container at room temperature. The small-molecule semiconductor 2,9-diphenyldinaphtho[2,3-b:2′, 3′-f]thieno[3,2-b]thiophene (DPh-DNTT; Nippon Kayaku, kindly provided by K. Ikeda[14]) was used as the active layer in the channel region of the TFTs and was deposited by thermal sublimation in vacuum (base pressure of 1×10^{-6} mbar) at a substrate temperature of 90 °C. For TC TFTs, the gold source and drain contacts were deposited directly onto the layer of DPh-DNTT using thermal evaporation in vacuum (base pressure of 1×10^{-7} mbar). The films in the channel region of the TFTs are shown in the scanning electron microscopy (SEM) images in Figs. 1(a) and 1(b).

In Fig. 1(c), a photograph of a fully fabricated BC TFT is shown. The flexible BC and TC organic TFTs were fabricated using a multi-finger layout, which is in principle the parallel connection of four identical TFTs. This layout helps us to provide sufficient mechanical stability of the stencil masks used for patterning[15] by keeping the size of the openings in the masks below a certain maximum independent of the channel width of the TFTs.



(a)



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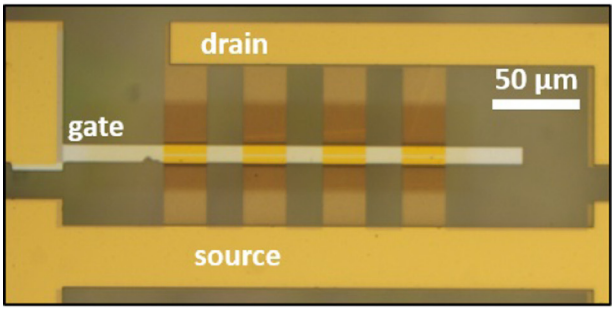

(c)

FIG. 1. (a) Scanning electron microscopy (SEM) image of the channel region of a BC TFT. (b) SEM image of the channel region of a TC TFT. (c) Photograph of an organic TFT fabricated in a multi-finger layout. The channel length is approximately 0.7 μm.

The critical dimensions of the TFTs (channel length and gate-to-contact overlaps) were measured using SEM. The measured gate-to-contact overlap lengths are listed in S4 and S5 in the supplementary material. The channel lengths of the transistors are approximately 0.7 μm and the sum of the finger widths is 100 μm, which is considered as the geometrical channel width ($W_{ch,SD}$). The gate-to-contact overlap lengths are varied asymmetrically with the sum of $L_{ov,GS}$ and $L_{ov,GD}$ held constant and equal to 10 μm.

All electrical measurements were performed at room temperature (292 K) in ambient air. Static transfer and output characteristics were measured using an Agilent 4156 C Semiconductor Parameter Analyzer and a custom LabView program. S-parameter measurements were performed using a Keysight N5231A Vector Network Analyzer and Cascade Microtech GS-SG $|Z|$ high-frequency probes.

III. SMALL-SIGNAL GAIN

A. Introductory information

The evaluation of the dynamic performance of any TFT technology generally starts by examining the small-signal current gain ($h_{21} = i_d/i_g$) as a function of the switching frequency (f) and the bias conditions.

This usually proceeds through an analysis of an equivalent small-signal circuit of the TFT (Fig. 2). From such an analysis, it is shown that h_{21} is dependent primarily on the channel transconductance (g_m) and the total gate capacitance encompassing the individual contributions from the source (C_{gs}) and drain (C_{gd}) sides of the TFT [Figs. 3(a) and 3(b)],[16]

$$h_{21} = \frac{g_m - j2\pi f C_{gd}}{j2\pi f\left(C_{gs} + C_{gd}\right)}. \tag{1}$$

This relatively simple equation provides a complete picture of the signal amplification properties of an *ideal* TFT. In practice, however, rather than a complete treatment of h_{21}, the figure of merit[18] that is most often reported for organic and other TFTs is the unity-current-gain cutoff (transit) frequency (f_T). This is defined as the frequency at which the absolute value of h_{21} is equal to unity. Using the Meyer capacitance model originally developed for ideal silicon metal-oxide–semiconductor field-effect transistors (MOSFETs),[19] f_T can, in principle, be estimated without the necessity of actually measuring h_{21}, but instead put in terms of

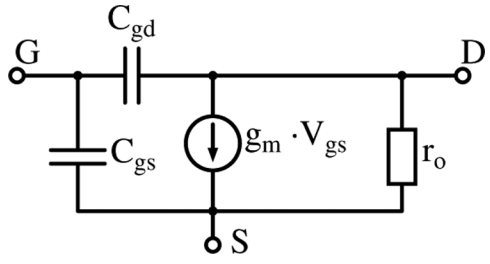

FIG. 2. Equivalent small-signal circuit of a field-effect transistor.

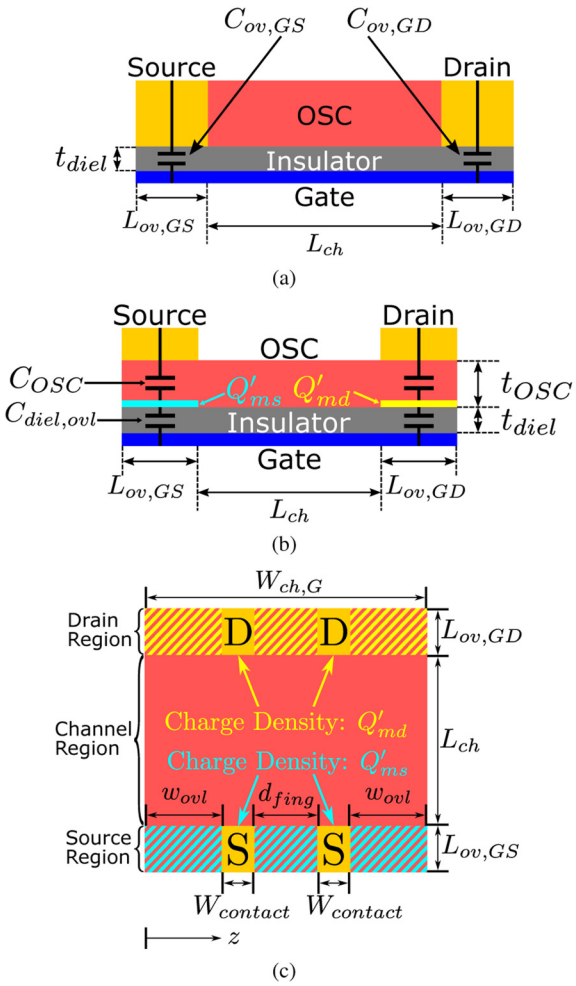

FIG. 3. (a) Schematic cross section of a bottom-contact (BC) organic TFT. (b) Schematic cross section of a top-contact (TC) organic TFT. Here, the semiconductor layer separates the source and drain contacts from the gate dielectric and thus from the gate-field-induced charge-carrier channel; hence, these transistors are also referred to as staggered TFTs. The overlap regions are assumed as a series connection of two capacitances. However, when the organic semiconductor (OSC) is operated in accumulation, the accumulation charges change the behavior of the series connection. The charge density at the source end of the channel is assumed to be found in the entire gate-to-source overlap region. Same considerations hold true for the drain side.[17] (c) Schematic top view of a BC TFT close to the gate dielectric surface. For the compact model, it is assumed that the charge density in the source region (which is the vicinity of the source contacts) is equal to the charge density at the source end of the channel. Same considerations hold for the drain region.

parameters that are controlled and measured through device engineering, including the channel length (L_{ch}), channel width (W_{ch}), and gate-to-contact overlap lengths ($L_{ov,GS}$, $L_{ov,GD}$), along with the DC bias conditions (gate-source voltage, V_{gs}, and drain-source voltage, V_{ds}), the area-normalized gate dielectric capacitance (C'_{diel}),

the threshold voltage (V_{T0}), and the effective charge-carrier mobility (μ_{eff}) in the semiconductor. For TFTs operated in the saturation regime ($V_{ds} \geq V_{gs} - V_{T0}$), f_T takes the form

$$f_T = \frac{\mu_{eff}(V_{gs} - V_{T0})}{2\pi L_{ch}\left(\frac{2}{3}L_{ch} + L_{ov,GS} + L_{ov,GD}\right)}. \quad (2)$$

The standard practice so far has been to use this equation to predict f_T for a given organic TFT technology from the measured DC transfer characteristics.

B. Special properties of organic TFTs

Even in state-of-the-art submicrometer-channel-length organic TFTs [Figs. 1(a)–1(c)], various non-idealities are present, which can drastically affect the adherence to this simple model. First, organic TFTs are plagued by exceptionally large contact resistances (R_C) between the source and drain contacts and the Organic semiconductor layer,[20] resulting in a reduction of μ_{eff} as L_{ch} is decreased. Theoretically, a reduction of μ_{eff} also leads to a reduction of f_T according to Eq. (2), but there is one significant aspect that is not captured by this equation: The inclusion of the contact resistance in terms of an effective mobility only captures the effect of a reduced DC current. However, as supported by Fig. 4, the density of quasi-mobile charges is altered by a contact resistance. Capacitance models for transistors, such as the Meyer model[19] used in Eq. (2), are usually based on an integration over this charge density. Consequently, the different charge densities due to contact resistances need to be taken into account for this integration and an effective mobility is not sufficient to accomplish this. Crucially, this directly limits the actual increase in f_T that would be otherwise expected from device miniaturization according to Eq. (2). Because of this potentially severe limitation, significant efforts in the research community have been focused on improving the contact-to-semiconductor interface to reduce R_C in organic TFTs. Recent breakthroughs in developing new materials[22,23] and novel TFT processing approaches[24] have led to organic TFTs with small width-normalized contact resistances ($R_C W$) of less than 100 Ω cm, in many cases reported along with measured transit frequencies of several tens of megahertz.[3,9,10,25] Table S2 in the supplementary material gives a literature summary of organic TFTs with measured transit frequencies of at least 3.5 MHz. In parallel to these advancements in device fabrication, properly accounting for the non-ideal contacts in organic TFTs has allowed circuit designers to implement organic TFTs more accurately in their designs.[26–30]

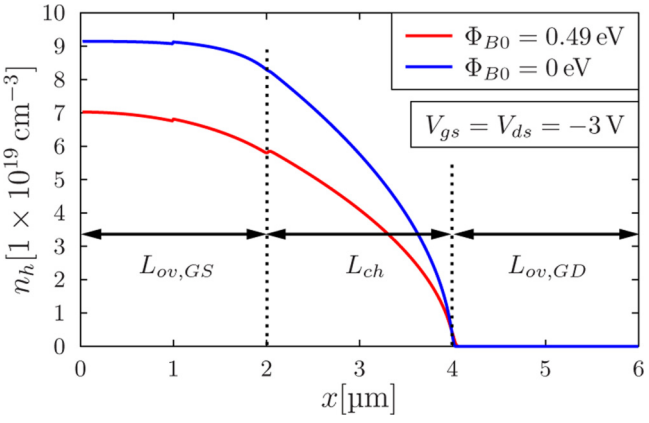

FIG. 4. Simulated density of quasi-mobile accumulated holes in a TC transistor along a cutline in the semiconductor in direct proximity to the gate dielectric. The results of a TCAD Sentaurus[21] simulation are shown. The red curve shows the results of a transistor with a work function mismatch between the source/drain electrodes and the organic semiconductor of 0.49 eV, whereas the blue curve shows the results of a transistor, where the work functions of the source/drain electrodes are aligned with the highest occupied molecular orbital (HOMO) of the organic semiconductor.

A second and equally critical aspect that is largely overlooked in the derivation of the simplified form for f_T in Eq. (2) is that it is explicitly assumed that the capacitance in both the channel region of the TFT and in the parasitic areas ostensibly defined by the gate-to-contact overlaps is simply determined by C'_{diel} and the physical dimensions of the TFT [Figs. 3(a) and 3(b)]. While this assumption can be made safely in, e.g., indium gallium zinc oxide (IGZO)-TFTs[31] and can at times be shown to provide an accurate description of some organic TFTs,[9] it is not generally applicable to organic TFTs of arbitrary geometries, but instead requires a more-detailed treatment using a compact model. Many such compact models for organic TFTs can be found in the literature (see Table S1 in the supplementary material); however, a more sophisticated approach is required to account for the additional influences from the voltage drop across the parasitic contact resistances, the frequency dependence of charges, and the charges in the fringe regions. Finally, an ideal approach should be able to capture the influences of the device fabrication details, including the choice of the device architecture, since both staggered and coplanar architectures are commonly used in organic TFTs [Figs. 3(a) and 3(b)].

We will provide solutions to these issues and will take into account the effects of the non-quasistatic effects of the charges, which occur when high frequencies are applied to the transistor terminals.

IV. COMPACT MODELING

In this section, the compact model for the analytical description of the small-signal gain h_{21} is presented. The model is based on quasistatic DC and AC models developed previously in the TH Mittelhessen group.

A. Quasistatic DC model

1. Basics

The compact model is based on the quasistatic DC model presented in Ref. 32, which will quickly be reviewed here. This is a charge-based model that provides a closed-form description for the density of quasi-mobile accumulation charges at the drain/source end of the channel,

$$Q'_{ms/d} = \frac{S}{\ln(10)} \cdot C'_{diel} \cdot \mathscr{L}\left\{\exp\left(\frac{V_{gs/d} - V_{T0}}{S_{sth}/\ln(10)}\right)\right\}, \quad (3)$$

where $\mathscr{L}$ is the first branch of the Lambert W function, C'_{diel} is the capacitance of the gate dielectric per gate area, and the parameters S_{sth} and V_{T0} are the sub-threshold swing and the threshold voltage, respectively. The model is originally formulated without the definition of a threshold voltage, but in order to facilitate the use of the model from the circuit designer's perspective, a threshold voltage based formulation is derived. The model accounts for the hopping transport in organic semiconductors by incorporating a field-dependent mobility,[33]

$$\mu = \kappa \cdot \left(\frac{Q'_{ms}}{C'_{diel}}\right)^{\beta}, \tag{4}$$

where $\kappa\,(\mathrm{cm}^2\,\mathrm{V}^{-\beta-1}\,\mathrm{s}^{-1})$ is a proportionality factor called the low-field mobility and β is the power-law factor. In addition, the model accounts for contact effects. It supports the inclusion of two types of contact resistances, namely, an Ohmic component ($R_{const}\,[\Omega]$) and a non-linear resistance ($R_{sb,s}\,[\Omega]$) arising from a Schottky barrier between the electrodes and the organic semiconductor at the source end of the channel. The Schottky barrier originates from the fact that the work function of the metal of the source/drain electrodes is not perfectly aligned with the highest occupied molecular orbital (HOMO) of the organic semiconductor. This work function mismatch is inevitable and is a limiting factor toward the TFT performance. The compact model includes the contact resistances by modifying the effective mobility following the procedure described in Ref. 30, which leads to the following expression for effective mobility:

$$\mu_{eff} = \frac{\mu}{1 + \mu \cdot \frac{W_{ch}}{L_{ch}} \cdot (R_{const} + R_{sb,s}) \cdot Q'_{ms}}. \tag{5}$$

The Ohmic part of the contact resistance is only geometry-dependent and not dependent on the voltages in the operation point. In coplanar (BC) transistors, R_{const} is simply a constant. By contrast, in staggered (TC) transistors, R_{const} is a function of the gate-to-source overlap length. The reason for this is that in a staggered architecture, the current density varies along the gate-to-source overlap length. The contact resistance is defined by the sheet resistance ($R_{sheet}\,[\Omega]$) of the organic semiconductor and the length of the gate-to-source overlap region. Following the procedure in Ref. 9, the Ohmic contact resistance for staggered (TC) transistors is calculated as follows:

$$R_{const} = 2 \cdot \frac{R_{sheet}}{W_{ch}} \cdot L_T \cdot \coth\left(\frac{L_{ov,GS}}{L_T}\right), \tag{6}$$

where L_T is the transfer length, in which 63% of the current is injected.

2. Workfunction mismatch

The work function mismatch at the electrode-to-channel junctions results in Schottky barriers, as stated above. The Schottky barrier at the source-to-channel junction is operated in the reverse direction, whereas the Schottky barrier at the drain-to-channel junction is operated in the forward direction. Consequently, the barrier at the source side imposes a notably higher contact resistance than the barrier at the drain side.

The non-linear resistance of the Schottky barrier at the source end of the channel ($R_{sb,s}$) is calculated following the procedure in Ref. 34. Applying a conformal mapping technique,[34] the electrical field at the source contact in the BC and TC transistors is calculated. Based on this, the effect of the Schottky barrier lowering due to image charges[18] is taken into account, resulting in a closed-form description of the Schottky barrier resistance $R_{sb,s}$. In Fig. 5, the schematic band diagram at the source contact is shown, which emphasizes the effect of Schottky barrier lowering. We will not present a full review of the model here. For a detailed description, the reader can refer to Ref. 34. This model eventually yields two values that are incorporated into the charge-based DC model,

$$R_{sb,s} = f\left(V_{gs}, V_{ds}, geometry, materials\right) \tag{7}$$

and

$$V_{sb,d} = f\left(V_{gs}, V_{ds}, geometry, materials\right). \tag{8}$$

$R_{sb,s}$ is the resistance of the reversely operated Schottky barrier at the source-to-semiconductor interface and $V_{sb,d}$ is the voltage drop over the forward-driven Schottky barrier at the drain-to-semiconductor interface. Both values are functions of the applied voltages, the device geometry, and the used materials. The resistance $R_{sb,s}$ is incorporated into the effective mobility according to Eq. (5). After the determination of $V_{sb,d}$, the charge density at the drain side is calculated again, but this time taking into account the voltage drop $V_{sb,d}$,

$$Q'_{md,barr} = \frac{S}{\ln(10)} C'_{diel} \mathscr{L}\left\{\exp\left(\frac{V_{gs} - V_{T0} - V_{ds} + V_{sb,d}}{S_{sth}/\ln(10)}\right)\right\}. \tag{9}$$

Finally, the drain current reads as follows:

$$I_{ds} = \mu_{eff} \cdot W_{ch} \cdot \left(\frac{k_B \cdot T}{q} \cdot \frac{Q'_{ms} - Q'_{md,barr}}{L_{ch}} + \frac{Q'^2_{ms} - Q'^2_{md,barr}}{2 \cdot L_{ch} \cdot C'_{diel}}\right) \times (1 + \lambda \cdot (V_{ds} - V_{dsx})), \tag{10}$$

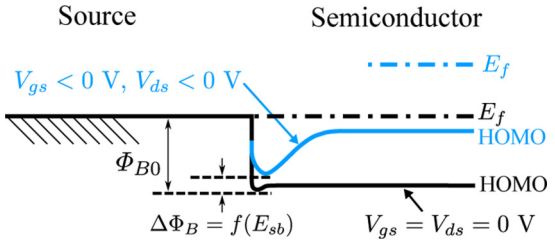

FIG. 5. Band diagram at the source-to-semiconductor interface, similarly as presented in Ref. 34. The short-channel DC model regards the non-linear resistance at the source end of the transistor as a reversely operated Schottky barrier, which is subject to a lowering due to image charges.

where λ is the channel length modulation factor. The voltage V_{dsx} is given by

$$V_{dsx} = \frac{1}{C'_{diel}} \cdot \left(Q'_{ms} - Q'_{md,barr}\right). \tag{11}$$

3. Fringing effects

The equation for the drain current neglects fringing effects so far. However, the drain current of a transistor with fringing regions could also be fitted using this equation. The fringing effects then lead to a mobility overestimation.[35] In Ref. 17, we have put special emphasis on the fringing regions. There, the effect of current spreading is taken into account by the definition of an effective gate width for the current,

$$W_{ch,eff} = \delta_{fit} \cdot (W_{ch,G} - W_{ch,SD}) + W_{ch,SD}, \tag{12}$$

where $\delta_{fit} \in [0, 1]$ is a fitting parameter and $W_{ch,G}$ is defined as

$$W_{ch,G} = N_{fing} \cdot W_{contact} + 2 \cdot w_{ovl} + \left(N_{fing} - 1\right) \cdot d_{fing}. \tag{13}$$

Here, N_{fing} is the number of fingers, w_{ovl} is the fringing width beyond the first and the last finger, $W_{contact}$ is the width of a single finger, $W_{ch,SD} = N_{fing} \cdot W_{contact}$ is the sum of the finger widths, and d_{fing} is the distance between the fingers, as can be seen in Fig. 3(c). In this equation, w_{ovl} is assumed to be symmetrically present at both ends of the transistor. However, for the equation, it is only important that $2 \cdot w_{ovl}$ equals the sum of the fringing widths beyond the first and the last electrode, even if these widths are asymmetrical. The effective gate width is used in the current equation, which then results in

$$I_{ds} = \mu_{eff} \cdot W_{ch,eff} \cdot \left(\frac{k_B \cdot T}{q} \cdot \frac{Q'_{ms} - Q'_{md,barr}}{L_{ch}} + \frac{Q'^2_{ms} - Q'^2_{md,barr}}{2 \cdot L_{ch} \cdot C'_{diel}}\right) \times (1 + \lambda \cdot (V_{ds} - V_{dsx})). \tag{14}$$

In the equation for the effective mobility [Eq. (5)], there also appears the channel width. Since the derivation of the effective mobility is based on the current equation, which in turn includes the effective channel width $W_{ch,eff}$, we also use $W_{ch,eff}$ in the effective mobility. By contrast, in the sheet resistance model according to Eq. (6), we use the geometric channel width $W_{ch,SD}$ as defined by the S/D electrodes.

There also exist other approaches to calculate the fringing currents by performing a conformal mapping of the transistor into a different geometry, where the current paths and accordingly the amount of fringing current can be calculated in a physics-based way.[36] However, since the separation between fringing currents and intrinsic channel currents is not crucial for the correct execution of the AC model, we will stick to our simple expression incorporating δ_{fit}.

4. De-coupling of the sub-threshold swing and the threshold voltage from the power-law mobility

The model incorporates a power-law mobility according to Eq. (4). In theory, this power-law mobility should only have an influence on the above-threshold characteristics of the transistor. However, it can be observed that there is an undesired influence of the power-law exponent β on the sub-threshold behavior and on the threshold voltage of the model's I/V characteristics. For a correct behavior of the compact model, it is mandatory that the modeled transfer characteristics exhibit the same sub-threshold swing and threshold voltage as the measured devices. In the supplementary material, we present a detailed analysis of the influence of the power-law exponent on the sub-threshold swing and the threshold voltage. The following equations can be derived for the de-coupling of the sub-threshold swing and the threshold voltage from the power-law exponent:

$$S_{sth} = S_{obs} \cdot (\beta + 1), \tag{15}$$

$$\Delta V_{T0} = \frac{S_{obs}}{\ln(10)} \cdot \ln\left((\beta + 1)^{\beta+1} \cdot \left(\frac{S_{obs}}{\ln(10)}\right)^{\beta}\right). \tag{16}$$

Here, S_{obs} is the sub-threshold swing that the model *really* exhibits and should agree to the measured swing. Parameter S_{sth} is the swing that has to be used internally as a model parameter so that the model exhibits S_{obs}. If, for example, $\beta = 0.5$ and we want the model to have a sub-threshold swing of 100 mV/dec, then we enter a swing of $S_{obs} = 100\,\mathrm{mV/dec}$, but internally, the model will use a value of $S_{sth} = 150\,\mathrm{mV/dec}$. The shift of the threshold voltage is included in the model by subtracting ΔV_{T0} from the measured threshold voltage that is entered as model parameter. The charge density at the source end of the channel then reads as follows:

$$Q'_{ms} = \frac{(\beta + 1) \cdot S_{obs}}{\ln(10)} \cdot C'_{diel} \cdot \mathscr{L}\left\{\exp\left(\frac{V_{gs} - V_{T0} + \Delta V_{T0}}{(\beta + 1) \cdot S_{obs}/\ln(10)}\right)\right\}. \tag{17}$$

The equation to describe the charge density at the drain end of the channel is modified equally.

B. Intrinsic charges

Based on the DC model described in the section before, we have already derived a quasistatic AC model accounting for both the intrinsic channel charges and parasitic charges in the overlap regions and for charges in fringing regions as well, which are present in organic TFTs fabricated in a multi-finger structure.[17]

The main points of this compact model are reviewed here in order to give a full picture. However, for a complete description, the reader can refer to Ref. 17. The intrinsic charges are calculated by integrating the charge density per gate area along the channel. Closely linked to the DC model,[32] some substitutions are performed, which lead to a closed-form equation for the total channel charge. Applying the well-known Ward–Dutton partitioning scheme,[37] the channel charges are separated into a portion belonging to the source terminal and a portion belonging to the drain terminal. The three charge integrals in their original form read

as follows:

$$Q_{c,orig} = W_{ch,G} \cdot \int_0^{L_{ch}} Q'_m(x)\, dx, \tag{18}$$

$$Q_{d,orig} = W_{ch,G} \cdot \int_0^{L_{ch}} \frac{x}{L_{ch}} \cdot Q'_m(x)\, dx, \tag{19}$$

$$Q_{s,orig} = W_{ch,G} \cdot \int_0^{L_{ch}} \left(1 - \frac{x}{L_{ch}}\right) \cdot Q'_m(x)\, dx, \tag{20}$$

where the following substitution is performed:

$$dx = -\left(\frac{W_{ch,eff} \cdot \mu_{eff}}{I_{ds}} \cdot Q'_m(x)\right) \cdot \left(\frac{\tilde{\alpha} \cdot V_{th}}{Q'_m(x)} + \frac{1}{C'_{diel}}\right) \cdot dQ'_m, \tag{21}$$

where $\tilde{\alpha}$ is the slope degradation factor, which due to the low influence of the sub-threshold regime on the channel charges can be set to unity, and $V_{th} = k_B T/q$. The variable x is expressed as

$$x = +\frac{W_{ch,eff} \cdot \mu_{eff}}{I_{ds}} \cdot \left[\tilde{\alpha} \cdot V_{th} \cdot Q'_m(x) + \frac{Q'^2_m(x)}{2 \cdot C'_{diel}}\right]_{Q'_m(x)}^{Q'_{ms}}. \tag{22}$$

Substituting the limits of integration by Q'_{ms} at position $x = 0$ and $Q'_{md,barr}$ at position $x = L_{ch}$ allows us to solve the three charge integrals analytically.

C. Short-channel extension for the AC model

The charge equations presented so far[17] are only valid for transistors that exhibit no or with respect to the intrinsic channel resistance negligible contact resistances. However, TCAD Sentaurus[21] simulations have revealed that the contact effects have an influence on the capacitances, especially if the contact resistances are high in contrast to the intrinsic channel resistance. In Fig. 4, the results of a TCAD Sentaurus simulation are depicted, where the density of quasi-mobile accumulated holes for a TC transistor is shown as a function of the position for a transistor with and a transistor without a Schottky barrier at the source/drain-to-channel junctions. The plot reveals that the charge densities are dependent on the barrier height and consequently on the contact resistance.

Here, we introduce an extension to the existing model. For the AC model, the transistor is modeled as a series connection of an inner transistor and contact resistances in form of lumped elements (see Fig. 6). Theoretically, from the DC model, the contact resistances R_{const} and $R_{sb,s}$ and also the voltage drop $V_{sb,d}$ over the Schottky barrier at the drain side are known. However, the purpose of the DC model is not an exact calculation of the different components of the contact resistance but a good reproduction of the current–voltage characteristics. Therefore, a deviation of the contact resistances from the values that they *really* have are not essential for a correct operation of the DC model. Investigations on TCAD Sentaurus simulations have shown that additional corrections are necessary. This leads us to the definition of a correction function f_{fit} and a distribution factor K_r which according to Fig. 6 modify

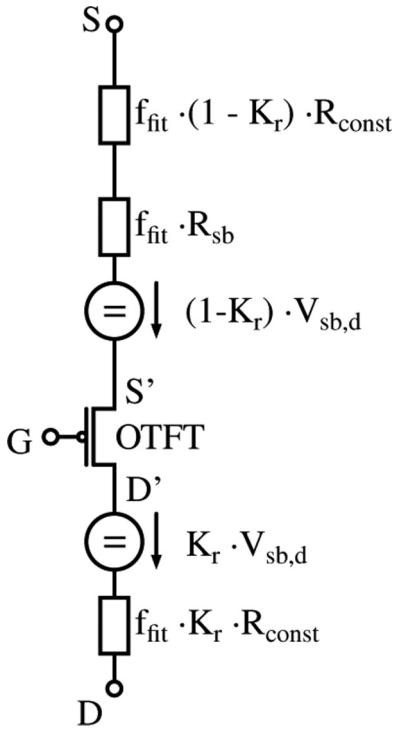

FIG. 6. Equivalent circuit for the AC operation of an organic TFT comprising contact resistances. The implementation of the short-channel DC model calculates the current including contact resistances in a closed form. For the AC model, the voltage drops over the contact resistances are needed explicitly.

the weight of the contact resistances and their distribution between the source and drain contact, respectively. Even if the voltage drop $V_{sb,d}$ is theoretically only present at the drain side of the transistor, we also allow this voltage do be attributed to both the source and drain sides. The function f_{fit} is defined as

$$f_{fit} = K_{fit} \frac{Q'_{ms} - Q'_{md,barr}}{Q'_{ms}}, \tag{23}$$

with K_{fit} being a fitting parameter. Q'_{ms} and $Q'_{md,barr}$ are the charge densities per gate area at the source and drain end of the channel, respectively, with the charge density at the drain side being reduced due to the voltage drop $V_{sb,d}$. If the transistor is operated in saturation, it means that $Q'_{ms} \gg Q'_{md,barr}$, since the channel is pinched off before the drain electrode. Consequently, f_{fit} becomes constant. In a strongly linear operation point, $Q'_{ms} \approx Q'_{md,barr}$, which causes f_{fit} to converge toward zero. This function has been determined based on the TCAD investigations. The parameter K_r allows for a redistribution of the influence of R_{const} and the voltage drop $V_{sb,d}$ (see Fig. 6). In the supplementary material, more information about the short-channel extension for the DC model is provided.

After the calculation of the DC current in any operation point, the voltage drops over the parasitic elements according to Fig. 6 can be determined by multiplying the modified contact resistances

by the DC current. The inner transistor thus has a lower gate-to-source voltage V_{gs}, and a lower drain-to-source voltage V_{ds}, than a transistor without contact resistances would have. We now use the reduced voltages to calculate the charge densities per gate area at the source/drain end of the channel *again*. For the AC model, we now use these charge densities that are different from the charge densities in the DC model.

D. Extrinsic charges

The intrinsic portion of the charges are calculated in the same manner for TC and BC transistors. However, there are stark differences in the extrinsic charges due to the overlap regions. In Fig. 3, 2D diagrams of the both transistor structures are shown. It can be seen that the overlap capacitances in the case of BC transistors are quite simple, since the source/drain electrodes are only separated from the gate electrode by the gate dielectric resulting in a first approximation in simple plate capacitors. By contrast, the TC transistors have a higher degree of complexity. The source/drain electrodes are separated from the gate electrode by a stack consisting of the organic semiconductor and the gate dielectric, which is, in principle, a series connection of two capacitors. In Ref. 17, the model for the overlap charges in TC transistors is presented.

In addition to the overlap charges, there are also charges in fringing regions. In our model, we assume that for both transistor architectures, the charge density per gate area at the drain/source end of the channel is also present in the whole region of the corresponding electrode [see Fig. 3(c), where a cutplane in a BC transistor is shown]. We can thus say that in the vicinity of the source fingers, the charge density per gate area is equal to the density of quasi-mobile accumulation charges at the source end of the channel (Q'_{ms}). Same considerations hold true for the drain side. Summing up the overlap charges and the fringing charges leads to the following expressions for the extrinsic charges in BC transistors:

$$Q_{ex,GS,BC} = C'_{diel} \cdot L_{ov,GS} \cdot N_{fing} \cdot W_{contact} \cdot V_{gs} + \left(2w_{ovl} + (N_{fing} - 1)d_{fing}\right) \cdot L_{ov,GS} \cdot Q'_{ms}, \quad (24)$$

$$Q_{ex,GD,BC} = C'_{diel} \cdot L_{ov,GD} \cdot N_{fing} \cdot W_{contact} \cdot (V_{gs} - V_{ds}) + \left(2w_{ovl} + (N_{fing} - 1)d_{fing}\right) \cdot L_{ov,GD} \cdot Q'_{md,barr}. \quad (25)$$

In TC transistors, the extrinsic charges also consist of two components: the geometric capacitance resulting from the stacking of the organic semiconductor and the gate dielectric and the additional capacitance due to accumulation charges. In contrast to BC transistors, the accumulation charges are present not only in the fringing regions between and beyond the fingers but also below the electrodes. With the definitions

$$C_{OSC} = \frac{\varepsilon_{OSC}}{t_{OSC}} \cdot L_{ov,GS/D} \cdot N_{fing} \cdot W_{contact}, \quad (26)$$

$$C_{diel,ov} = C'_{diel} \cdot L_{ov,GS/D} \cdot N_{fing} \cdot W_{contact}, \quad (27)$$

where $L_{ov,GS/D}$ is the corresponding gate-to-contact overlap length at the source or drain side, the extrinsic charges in TC transistors can be derived as[17]

$$Q_{ex,GS,TC} = \frac{C_{diel,ov} \cdot C_{OSC}}{C_{diel,ov} + C_{OSC}} \left(V_{gs} - \frac{Q'_{ms}}{C'_{diel}}\right) + W_{ch,G} Q'_{ms} L_{ov,GS}, \quad (28)$$

$$Q_{ex,GD,TC} = \frac{C_{diel,ov} \cdot C_{OSC}}{C_{diel,ov} + C_{OSC}} \left(V_{gs} - V_{ds} - \frac{Q'_{md,barr}}{C'_{diel}}\right) + W_{ch,G} Q'_{md,barr} L_{ov,GD}, \quad (29)$$

where $W_{ch,G}$ is defined according to Eq. (13).

E. Non-quasistatic effects

Previously, we have assumed that the density of quasi-mobile accumulation charges is nearly constant for any point along the z-axis of the device.[17] The z-axis points in the direction of the channel width, as shown in Fig. 3(c). For the quasistatic case, this assumption may hold true, but in a non-quasistatic operation, the location of the charges is important. Accumulation charges cannot be created or disappear by recombination within the organic semiconductor. They have to enter or leave the device through the source and drain electrodes. Consequently, points farther away from the electrodes cannot be charged or discharged as easily as points closer to the electrodes. In particular, the charges in the fringing regions are subject to a slower charging and discharging, because they are located beyond the channel center. We thus model the frequency dependence of the charges by decreasing the width of the fringing regions, which we take into account for the charge calculation. This is accomplished by a scaling function, which is defined in analogy to Ref. 38 as follows:

$$C_{scale} = C_{scale,high} + \frac{C_{scale,low} - C_{scale,high}}{(1 + f \cdot \tau_{scale})^{p_{scale}}}. \quad (30)$$

C_{scale} converges to $C_{scale,low}$ for low frequencies and to $C_{scale,high}$ for high frequencies. The parameter τ_{scale} controls the transition from the low-frequency value to the high-frequency value and p_{scale} is the exponent of the denominator, which also controls the steepness of the transition. C_{scale} is plotted over the frequency for a specific set of parameters in Fig. 7(a). If $C_{scale} = 1$, all fringing regions are accounted for, see Fig. 7(b). For $C_{scale} = 0$, only the channel region defined by the source/drain contacts is accounted for. The function C_{scale} is incorporated in the equations for the total charges.

In addition to the charges in fringing regions, the charges also in the intrinsic channel regions and, in case of TC transistors, the accumulation charges in the gate-to-contact overlap regions exhibit a frequency dependence. We assume that the frequency dependence of these charges is not necessarily the same as for the fringe charges. Therefore, we define a second scaling function of exactly the same structure as for the fringe charges,

$$C_{scale2} = C_{scale2,high} + \frac{C_{scale2,low} - C_{scale2,high}}{(1 + f \cdot \tau_{scale2})^{p_{scale2}}}. \quad (31)$$

The intrinsic channel charges in TC and BC transistors and also the overlap accumulation charges in TC transistors are multiplied

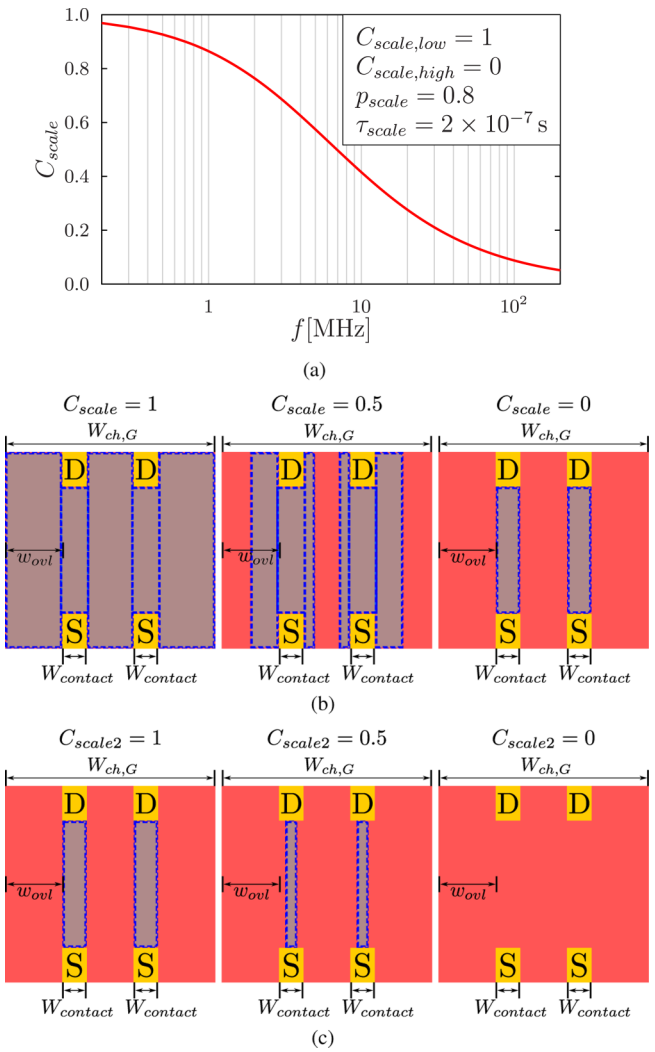

FIG. 7. (a) Shape of the function C_{scale} for a certain set of parameters. (b) Illustration of the fringing areas that are used for the charge calculation depending on the value of C_{scale}. If $C_{scale} = 1$, all of the fringing charges are used for the charge calculation. If $C_{scale} = 0$, only the intrinsic and overlap charges are used, whereas the fringing regions are neglected. (c) Illustration of the influence of the function C_{scale2} on the charges. We note that this function is an empirical approach that does not necessarily reflect the true charge distribution around the electrodes.

by this scaling function C_{scale2}. Figure 7(c) visualizes the influence of C_{scale2} as an effective channel width, which is used for the charge calculation. We note that this is an empirical approach since, in principle, a higher frequency leads to a reduction of the area around the electrodes, which are modulated by the applied signal. Theoretically, this would result in a reduction of the channel length. However, due to the very short channels in comparison to the large gate-to-contact overlap regions, we do not treat the intrinsic channel charges in more detail. Since C_{scale2} is a factor in the charge equations, its influence can be visualized by a reduction of the channel width. With the definitions of C_{scale} and C_{scale2}, the equations for the total charges and for the extrinsic charges are changed. The intrinsic channel charge then reads as follows:

$$Q_c = \left(C_{scale}\left(2w_{ovl} + \left(N_{fing} - 1\right)d_{fing}\right) + C_{scale2}N_{fing}W_{contact}\right) \times \int_0^{L_{ch}} Q'_m(x)\,dx. \tag{32}$$

The charge equations for Q_d and Q_s [Eqs. (19) and (20)] are modified in the same way. The equations for the extrinsic charges are modified as well, which in case of the BC transistors lead to the following equations:

$$Q_{ex,GS,BC} = C'_{diel}L_{ov,GS}N_{fing}W_{contact}V_{gs} + C_{scale}\left(2w_{ovl} + (N_{fing} - 1)d_{fing}\right)L_{ov,GS}Q'_{ms}, \tag{33}$$

$$Q_{ex,GD,BC} = C'_{diel}L_{ov,GD}N_{fing}W_{contact}(V_{gs} - V_{ds}) + C_{scale}\left(2w_{ovl} + (N_{fing} - 1)d_{fing}\right)L_{ov,GD}Q'_{md,barr}. \tag{34}$$

The extrinsic charges in case of the TC transistors change to the following formulation:

$$Q_{ex,GS,TC} = \frac{C_{diel,ov}C_{OSC}}{C_{diel,ov} + C_{OSC}}\left(V_{gs} - \frac{Q'_{ms}}{C'_{diel}}\right) + \left[C_{scale}\left(2w_{ovl} + \left(N_{fing} - 1\right)d_{fing}\right) + C_{scale2}N_{fing}w_{fing}\right]Q'_{ms}L_{ov,GS}, \tag{35}$$

$$Q_{ex,GD,TC} = \frac{C_{diel,ov}C_{OSC}}{C_{diel,ov} + C_{OSC}}\left(V_{gs} - V_{ds} - \frac{Q'_{md,barr}}{C'_{diel}}\right) + \left[C_{scale}\left(2w_{ovl} + \left(N_{fing} - 1\right)d_{fing}\right) + C_{scale2}N_{fing}w_{fing}\right]Q'_{md}L_{ov,GD}. \tag{36}$$

In the literature, there also exist more sophisticated approaches for the calculation of the frequency dependence of, for example, metal-insulator–semiconductor (MIS) capacitors[39] or the flow of charges in a transistor using the current continuity equation.[40] However, the results show that our approach is sufficient to capture the frequency effects.

F. Small-signal gain

Based on the modeling work presented so far, we now have a full compact model that can be used to calculate the small-signal gain h_{21}. For this equation, the transconductance g_m and the capacitances C_{gs} and C_{gd} are needed. These values are obtained by numerically deriving the drain current and the total charges with respect to the voltages in the operation point. There is one more fact to be discussed when looking at the equation for the small-signal gain: Here, the capacitances C_{gs} and C_{gd} are used. However, the capacitances in transistors are generally not reciprocal,[41] which means for instance that $C_{gs} \neq C_{sg}$. In principle, it is thus not allowed to imagine the transistor capacitances as lumped elements, such as it is done in Fig. 2. However, because of the small channel length in comparison to the gate-to-contact overlap lengths, the

extrinsic overlap capacitances of the transistors under investigation dominate over the intrinsic channel capacitances. Since the non-reciprocity of the capacitances is only important for the intrinsic channel capacitances, we can say that the transistors in this work will show almost reciprocity, which allows us to say that $C_{gs} \approx C_{sg}$ and $C_{gd} \approx C_{dg}$. We now have a full analytical expression for h_{21} which we will verify in Sec. V.

V. MODEL VERIFICATION

A. Quasistatic DC model

In this section, the fitting procedure of the quasistatic DC and AC models for the TC and BC transistors is presented. The DC transfer and output characteristics of all TFTs were measured and subsequently examined using our compact model. The transistors under investigation here show very low process variability. However, in order to model h_{21} properly, every transistor undergoes a DC fitting procedure. Typical process and device parameters, such as the channel length, the threshold voltage, the sub-threshold swing, and the Schottky barrier parameters, are determined for each transistor so that the compact model agrees with the DC transfer and output characteristics.

All TFTs examined here have the same channel length (approximately 0.7 μm) and the same total gate-to-contact overlap length (sum of the gate-to-source and gate-to-drain overlap lengths, $L_{ov,GS} + L_{ov,GD}$; approximately 10 μm), but the overlaps are asymmetric, i.e., $L_{ov,GS}$ varies between 1 and 9 μm (and $L_{ov,GD}$ accordingly between 9 and 1 μm). In Fig. 8, the measured gate-to-contact overlap lengths are depicted, proving the quality of the fabrication process.

Tables S3–S5 in the supplementary material specify the fitting parameters, which were chosen for the TFTs. In Figs. 9(a)–9(d), we show example fits to the measured transfer and output curves, demonstrating the agreement that is obtainable when the contact resistance and barrier-lowering effects are considered. Deviations in the current–voltage characteristics at small drain-source voltages do not diminish the results of this work, since the quality of fit at the operation point $V_{gs} = V_{ds} = -3$ V, which is used for the small-signal measurement, is very good. Figure 9(e) shows the measured width-normalized transconductances of the fabricated transistors. We find that the transconductances of the staggered (top-contact, TC) TFTs [Fig. 3(b)] show a systematic decrease for $L_{ov,GS}$ smaller than the transfer length (L_T), which is directly related to the contact resistance,[42] since injection becomes limited by the transfer length (L_T) at such small overlaps in staggered architectures.[9,43] This agrees with the transmission line method (TLM) analysis that yielded $L_T = 1.4\,\mu$m, which was also close to our previous report for similarly fabricated TC TFTs in which the transfer length was found to be 2.4 μm.[44] For $L_{ov,GS} > L_T$, the transconductance of the TC TFTs is essentially independent of the overlap asymmetry. In coplanar (bottom-contact, BC) TFTs [Fig. 3(a)], the transconductance is found to be generally larger than in TC TFTs by a factor of 2.5 to 3, with no discernible dependences on the gate-to-contact overlaps, but with a broader distribution than in TC TFTs. We note that there is one outlier in the set of BC TFTs ($L_{ov,GS} = 6.5\,\mu$m), which shows $g_m/W = 2.5\,\mathrm{S\,m^{-1}}$, more than 50% smaller than the transconductances of the other BC TFTs with g_m/W between 5.2 and 6.0 $\mathrm{S\,m^{-1}}$. The associated h_{21} data show a much lower small-signal gain, as expected. The reason for the higher transconductance in BC transistors is their lower $R_C W$ (35 Ω cm) and larger intrinsic channel mobility ($\mu_0 = 4.3\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$), determined by the TLM analysis as reported in Ref. 10. The TLM analysis of the TC TFTs yields $R_C W = 61\,\Omega$ cm and $\mu_0 = 2.7\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (see Fig. S4 in the supplementary material).

Similar to our previous reports,[10,44] the BC TFTs exhibit a much steeper subthreshold swing compared to the TC TFTs.[45] Here, the BC TFTs show subthreshold swings of about 70 mV/dec, whereas the TC TFTs have values of about 230 mV/dec.

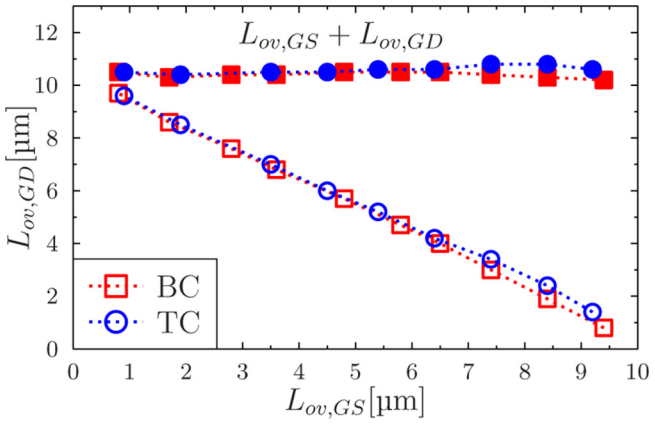

FIG. 8. Diagram of the measured gate-to-contact overlap lengths. $L_{ov,GD}$ is shown over $L_{ov,GS}$, proving that the process is well controlled. As the plot depicts, the sum of both overlap lengths is nearly constant and equal to 10 μm.

B. AC characteristics of submicrometer-channel-length organic TFTs

1. General investigations

S-parameters were measured while applying DC voltages ($V_{gs} = V_{ds} = -3$ V) using superimposed small-signal voltages $v_{gs} = v_{ds} = 0.2$ V. Having a threshold voltage of approximately $V_{T0} = -0.8$ V, under these conditions, the TFTs are operated entirely within the saturation regime. h_{21} was calculated from the S-parameter data by performing standard conversions according to Ref. 46. The compact model was fitted to the data by determining parameters for the small-signal models (i.e., values for the fitting parameters of C_{scale} and C_{scale2}) and for the short-channel AC model. Tables S3–S5 in the supplementary material show the chosen values for these parameters.

In Figs. 10(a) and 10(b), the compact modeling results (solid lines) are shown in comparison to the measured absolute values of h_{21} (dotted lines). The data are shown for all of the transistors with the different gate-to-contact overlap lengths. Here, the sum of $L_{ov,GS}$ and $L_{ov,GD}$ is kept constant at 10 μm, with $L_{ov,GS}$ varying from 1 to 9 μm. Owing to the larger transconductances as a result of the smaller contact resistance, the BC TFTs generally show higher h_{21} than the TC TFTs. Through comparison of the frequency

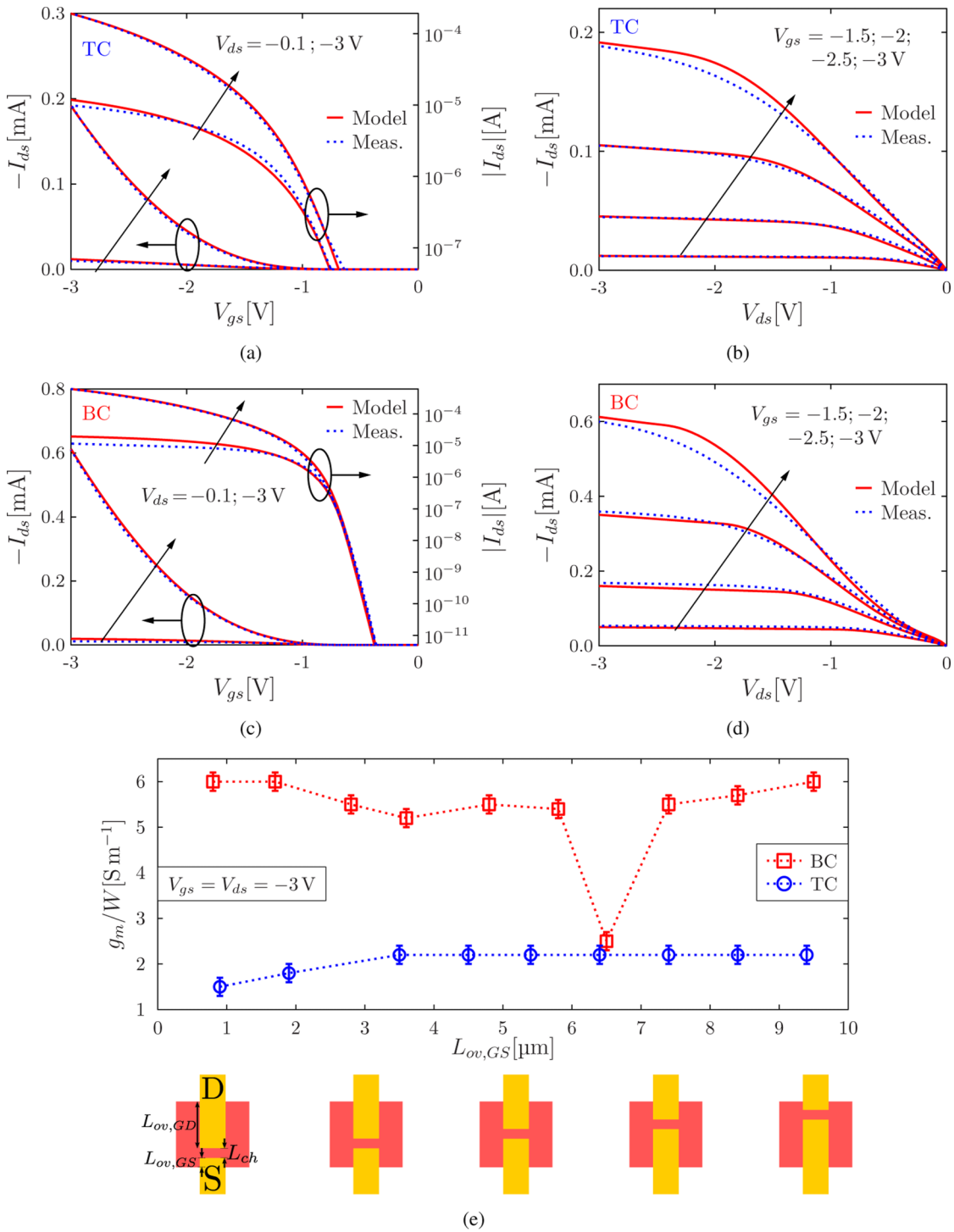

FIG. 9. (a) Transfer and (b) output characteristics of a TC TFT with $L_{ov,GS} = 5.4\,\mu$m, $L_{ov,GD} = 5.2\,\mu$m, and $L_{ch} = 0.67\,\mu$m. (c) Transfer and (d) output characteristics of a BC TFT with $L_{ov,GS} = 7.4\,\mu$m, $L_{ov,GD} = 3.0\,\mu$m, and $L_{ch} = 0.66\,\mu$m. (e) Width-normalized transconductance of all TFTs included in the analyses. The transconductance was measured at $V_{gs} = V_{ds} = -3\,$V and normalized with respect to the sum of the individual finger widths (100 μm). The pictogram shows the asymmetry between $L_{ov,GS}$ and $L_{ov,GD}$.

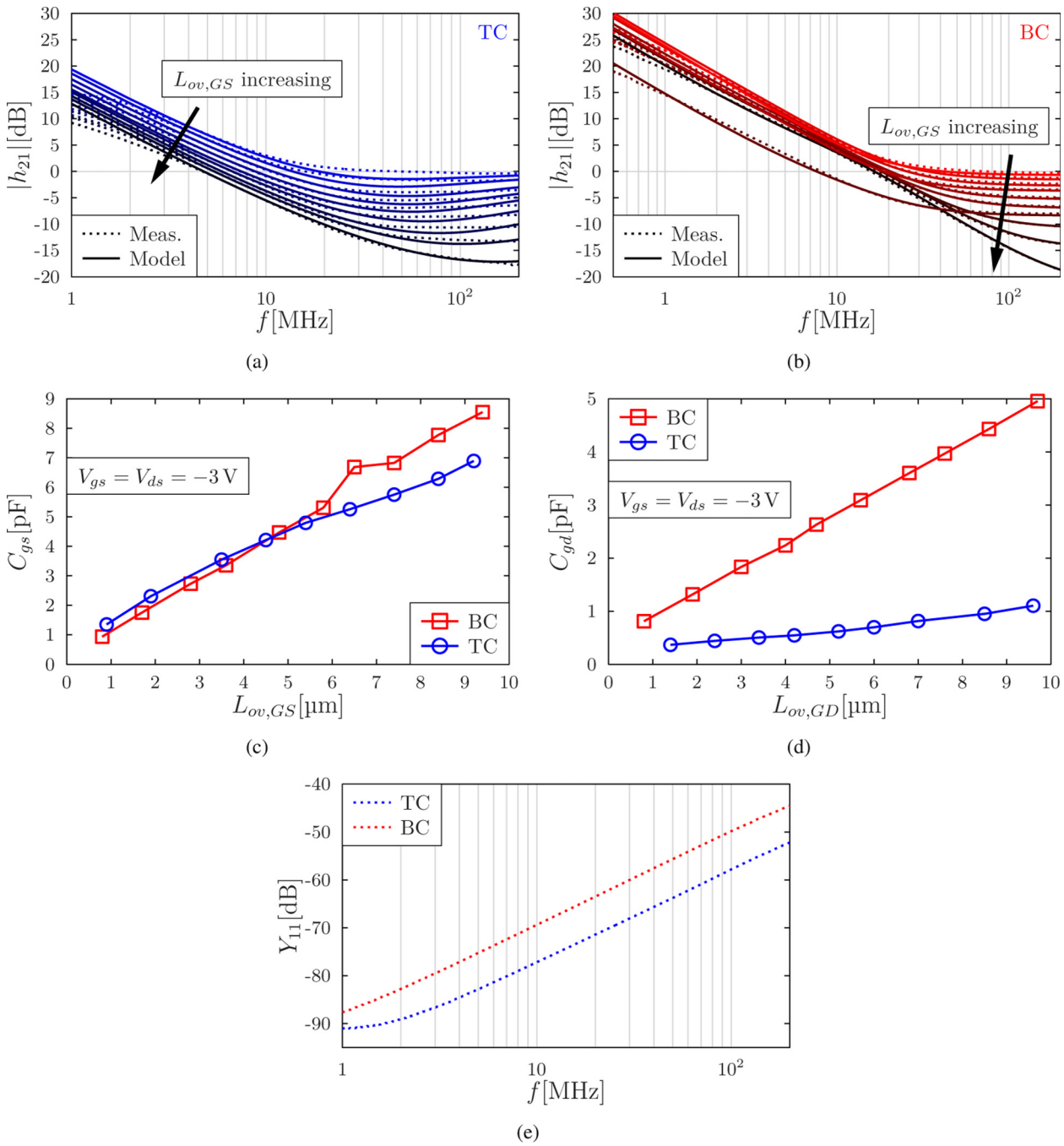

FIG. 10. (a) Small-signal gain (h_{21}) for the TC TFTs and (b) BC TFTs. The measurements are depicted as solid lines, and the compact model results are shown as dotted lines. For low frequencies, the measurement system is operated close to its resolution limit, which is the reason for the slightly visible saturation of h_{21} for low frequencies. (c) Quasistatic gate-source capacitance (C_{gs}) in TC and BC TFTs calculated using the compact model and plotted against the measured gate-to-source overlap length ($L_{ov,GS}$). For each $L_{ov,GS}$, the quasistatic gate-source capacitance (C_{gs}) of the TC TFTs is nearly identical to that of the BC TFTs, despite the differences in device architecture. (d) Quasistatic gate-drain capacitance (C_{gd}) calculated using the compact model. In contrast to C_{gs}, the quasistatic gate-drain capacitance C_{gd} of the TC TFTs is notably smaller than that of the BC TFTs due to the presence of the depleted organic semiconductor layer between the drain contact and the gate dielectric. (e) Measured small-signal admittance parameters (Y_{11}) of the TFTs with the smallest $L_{ov,GS}$ for each architecture, highlighting the difference in the overall capacitance between TC and BC TFTs.

dependence of h_{21}, there is a strong indication that the TC TFTs show a much greater dependence of h_{21} on the asymmetry of the gate-to-contact overlap lengths. Given that the transconductance of the TC TFTs is mostly constant except for the two TFTs with the smallest $L_{ov,GS}$, the influence of the gate-to-contact overlap asymmetry on the small-signal gain is more likely linked to the extrinsic capacitances that vary between the two transistor architectures. In principle, the gate electrode is coupled to the drain and source contacts only through the capacitances C_{gs} and C_{gd}, which causes h_{21} to approximately follow a trend of $-20\,\mathrm{dB/dec}$ well below the transit frequency.[15,16,47] The slightly visible formation of a plateau in the measured h_{21} for low frequencies can be explained by the properties of the measurement system. In the section "Vector Network Analyzer" in the supplementary material, we provide more details about that.

2. Analysis of the source side

We focus our analysis first on the source side of the transistors. Under the DC bias conditions applied here ($V_{gs} = V_{ds} = -3$ V), the organic semiconductor regions at the source side of the TFTs are operated in strong accumulation. Since the contacts in BC TFTs are directly interfacing the gate dielectric, they behave to a first approximation like simple parallel-plate capacitors with the capacitance C'_{diel}, showing limited frequency dependence due to a minor change in the permittivity of the gate insulator.[38,39] In Fig. 11, the measured capacitance of the gate dielectric is shown, proving that there is only a small change of less than 5%. In both architectures, the organic semiconductor layer that extends outside of the intrinsic channel region and the area defined by the contacts must be considered [Fig. 3(c), indicated by the red/cyan region in the diagram], since this region will have a potentially significant impact in the form of a parasitic fringe capacitance due to accumulated charge carriers. A change in $L_{ov,GS}$ changes the total area of this region, such that the amount of accumulated charges also changes. However, one key difference between the two architectures is that in TC TFTs, the accumulation of charges also takes place in the organic semiconductor layer between the contact and the gate dielectric [Fig. 3(b)]. Thus, a change in $L_{ov,GS}$ changes the charge accumulation in the overlap regions in the TC TFTs as well. Even so, in strong accumulation, the surface potential in the organic semiconductor is nearly constant, so that the voltage drop over the geometric series connection of the gate dielectric capacitance and the capacitance of the semiconductor in TC transistors is also nearly constant. The consequence is that in strong accumulation, the capacitance of the overlap region in TC transistors is entirely defined by the accumulated charges and no longer by the stacking of the two geometric capacitors. Furthermore, in strong accumulation, the density of accumulated charges follows the trend $Q'_{ms} = C'_{diel}(V_{gs} - V_{T0})$ (see Ref. 32), where V_{T0} is the threshold voltage. As Q'_{ms} is proportional to the gate dielectric capacitance (C'_{diel}), both the effective overlap capacitance in TC transistors and also the fringing capacitance in TC and BC transistors are determined entirely by C'_{diel} [see section "MIM vs MISM" in the supplementary material for an illustrative comparison between a simulated Metal-insulator–metal (MIM) and metal-insulator–semiconductor–metal (MISM) structure]. This point is further illustrated in Fig. 10(c) by the quasistatic C_{gs} that was determined using the compact model. In spite of the differences, both device architectures exhibit similar quasistatic C_{gs} in the chosen operation point.

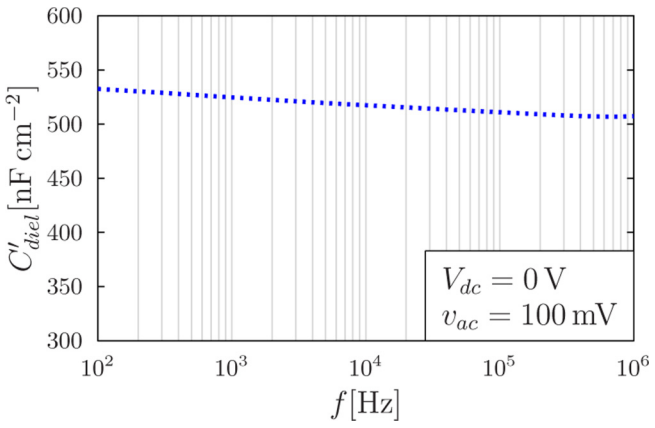

FIG. 11. Measured dielectric capacitance per area of the gate dielectric (aluminum oxide and self-assembled monolayer of *n*-tetradecylphosphonic acid).

3. Analysis of the drain side

At the drain side, the differences between the two architectures become more substantial.[48] Since the gate-drain voltage is nearly zero under the chosen bias conditions, the organic semiconductor in the drain region is operated in the depletion mode. The density of accumulated charges is then also nearly zero, and any change of the yellow/red area in Fig. 3(c) by a change in $L_{ov,GD}$ will not lead to a change in the accumulated charges in the fringe regions surrounding the drain contact. Furthermore, due to the saturation of the intrinsic channel, the drain potential has almost no control over the intrinsic channel charges and, consequently, the overlap charges are the only contributors to the gate-drain capacitance (C_{gd}). The depleted organic semiconductor in this case behaves like an insulator, so that in the TC TFTs, the overlap capacitance (C_{gd}) is given by the geometric series connection of the gate dielectric and the depleted organic semiconductor layer defined by the dimensions of the drain contact. This capacitance is thus significantly smaller than C_{gd} in comparable BC TFTs, where C_{gd} only contains a contribution from the gate dielectric. This is verified with simulated C_{gd} values, which for such a quasistatic case are plotted in Fig. 10(d). Indeed, the TC TFTs exhibit an overall smaller and more constant C_{gd}, while in BC TFTs, the change in C_{gd} with respect to a change in $L_{ov,GD}$ is more pronounced.

4. Discussion

Taking this all into account, it is apparent why the parasitic capacitances and, therefore, the total admittance [$Y_{11} = j2\pi f(C_{gs} + C_{gd})$] between the gate electrode and the source and drain contacts is larger in the BC TFTs than in the TC TFTs [Fig. 10(e)]. This might lead to the conclusion, by virtue of the smaller capacitance, that the TC TFTs have a potential for achieving higher gain at higher frequencies for smaller $L_{ov,GS}$ than

otherwise equivalent BC TFTs. However, due to the strong dependence of charge injection on the transfer lengths in TC TFTs, a significant down-scaling of $L_{ov,GS}$ decreases the transconductance, negating any potential benefits related to the capacitance reduction [Fig. 9(e)]. BC TFTs, by contrast, show a much weaker dependence of h_{21} on the degree of asymmetry of the gate-to-contact overlap lengths overall, even if the capacitances are larger than those of TC TFTs. Nonetheless, in principle, it can also be expected that a smaller $L_{ov,GS}$ (and in this case a simultaneously larger $L_{ov,GD}$) will result in a higher small-signal gain for both architectures, since capacitances still make a contribution on the source side of the contacts in BC TFTs.

As mentioned above, the unity-gain cutoff (transit) frequency is often used as the figure of merit for the description of the small-signal behavior of transistors. However, upon observation of the simulated and measured curves for h_{21} shown in Fig. 10, it becomes evident that the definition of the transit frequency can draw a distorted picture of the small-signal amplification behavior of the organic TFTs in which $L_{ov,GS} \ll L_{ov,GD}$. The main issue is that the change in the level of saturation of h_{21} at high frequencies for TFTs with the shortest $L_{ov,GS}$ results in the intersection point of h_{21} with the zero-dB axis shifting to a region where h_{21} exhibits a slope significantly smaller than -20 dB/dec. According to the usual definition for f_T, the TC TFT with the shortest $L_{ov,GS}$, for example, would yield a transit frequency of $\approx$47 MHz, even though the gain is severely reduced for frequencies well below this value. From the circuit designer's perspective, it would make more sense to extrapolate the curve from the -20 dB/dec-region to the zero-dB axis. This leads to a transit frequency of 15 MHz for the best TC transistor and to 21 MHz for the best BC transistor (as reported in Ref. 10), which are the highest transit frequencies reported for low-voltage organic TFTs to date.

VI. CONCLUSION

We have demonstrated a detailed analysis of the effects of non-idealities in the design of organic TFTs on the small-signal gain, the key parameter of interest for the development of organic TFTs suitable for high-frequency applications. We implemented a compact model that can accurately capture the DC and AC characteristics of organic TFTs fabricated in both coplanar (BC) and staggered (TC) architectures with submicrometer-channel lengths. This allowed us to perform a detailed probe into the effects of un-patterned organic semiconductor layers and asymmetric gate-to-contact overlaps, which can be a major source of non-ideality in the AC performance characteristics. Our observations show that even though the capacitances in BC TFTs are generally higher than in TC TFTs, a higher small-signal gain with a considerably weaker dependence on asymmetry in the parasitic gate-to-contact overlap capacitances can be realized. We attribute this to the notably larger transconductance due to smaller contact resistance than in TC TFTs.

SUPPLEMENTARY MATERIAL

In the supplementary material, we provide an overview over the state of the art including an overview over different compact models for organic TFTs and a summary of different organic TFTs for which in the literature a transit frequency of at least 3.5 MHz has been reported. Furthermore, we show the derivation of the equations for the de-coupling of the sub-threshold swing and the threshold voltage from the power-law mobility in the compact model. Then, we explain the fitting procedure of the compact model and provide tables showing the chosen fitting parameter values. Additionally, we show the results of the TLM analysis for the TC transistors, some more background information about the measurement system, and an illustrative comparison of the capacitive behavior of a metal-insulator–metal and a metal-insulator-semiconductor–metal interface.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supplementary Material - Flexible megahertz organic transistors and the critical role of the device geometry on their dynamic performance

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STATE OF THE ART

In this section, we will give an overview over the state of the art regarding compact models for the AC behavior of OTFTs. In addition to new materials design and engineering approaches, the successful implementation of organic TFTs into high-frequency circuits requires accurate physics-based models of their performance characteristics. There exists a variety of compact DC models incorporating effects such as non-linear contact resistances, a power-law mobility etc. for organic TFTs[1–9]. In addition, there has been some development of compact models addressing the AC characteristics of organic TFTs[7,9–18]. However, none of these fully account for various non-idealities that can arise in organic TFTs[19]. Table S1 gives an overview over the state of the art of compact AC models found in literature and their capabilities. Many models can address some of the aspects which are important for organic TFTs, but modeling and explaining the structure-dependent differences in h_{21} is not possible with these models. Here, we present a comprehensive model to fully characterize the small-signal current gain (h_{21}) devoloped with the support of measurement data from state-of-the-art high-frequency organic TFTs fabricated on flexible substrates, operating at low voltages and with sub-micron channel lengths[20]. To our knowledge, our model is the first to fully capture the influences on the gain of the device architecture (TC vs. BC or staggered vs. coplanar) which directly affects the parasitic capacitances and the contact resistance. This development will broadly impact both the device modeling community as well as groups actively working on designing circuits based on organic TFTs and other non-ideal transistors for high-frequency applications. In addition to the state of the art regarding compact models for the DC and AC performance, we also provide an overview over the state of the art regarding the dynamic performance of organic thin-film transistors. Table S2 gives an overview over organic thin-film transistors for which in the literature a transit frequency of at least 3.5 MHz has been reported.

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DE-COUPLING OF THE SUB-THRESHOLD SWING AND THE THRESHOLD VOLTAGE FROM THE POWER-LAW MOBILITY

The quasistatic DC model incorporates a power-law mobility according to Eq. (4) in the main document. In theory, this power-law mobility should only have an influence on the above-threshold characteristics of the transistor. However, it can be observed that there is an undesired influence of the power-law exponent β on the sub-threshold behavior. This problem is visualized in Fig. S1(a), where the transfer curves of three transistors are shown. The transistors have the same set of fitting parameters, but the power-law exponent β differs. It becomes clearly visible that β changes the sub-threshold swing of the compact model. The model no longer exhibits the sub-threshold swing which is set by the parameter S_{sth}. For convenience, we will omit the suffix "sth" and talk only of S. A compensation of the influence of the power-law mobility exponent β on the sub-threshold swing has to be found. To start with, we firstly focus on the mobility. According to Eq. (5) in the main document, the mobility incorporates the contact resistances $R_{sb,s}$ and R_{const}. Since in the deep sub-threshold regime of operation, the charge density Q'_{ms} becomes very small, the contact resistances almost have no influence. Thus, the effective mobility in the off-state is only defined by the power-law mobility:

$$\mu_{OFF} = \kappa \cdot \left(\frac{Q'_{ms,OFF}}{C'_{diel}} \right)^{\beta}, \tag{1}$$

where $Q'_{ms,OFF}$ is Q'_{ms} in the Off-state. Next, we will focus on the charge density Q'_{ms} according to Eq. (3) in the main document. In the sub-threshold regime of operation, where $V_{gs} < V_{T0}$, the argument of the exponential function becomes negative. Thus, the exponential function yields a value between zero and one, converging to zero, when V_{gs} becomes smaller. Thus, the Lambert W function is evaluated at a point very close to zero. Please recall that the Lambert W function is the inverse function of the problem

$$y = x \cdot \exp(x). \tag{2}$$

Since this cannot be analytically solved for x, the Lambert W function is defined, which is solved numerically, for example by a Taylor series:

$$x = \mathscr{L}(y). \tag{3}$$

TABLE S1. Benchmarking of compact AC models

	Castro-Carranza	Marinov-Deen	Valletta	Torricelli	Zaki (Meyer model)	Different other approaches	Our model
charge-based	no	no	no	yes	no	no	yes
closed-form	yes	yes	no	yes	yes	only[16,17]	yes
combined DC and and AC model	yes	yes	yes	yes	no	only[9,16,18]	yes
overlap charges for TC architecture	no	yes, with extension[21]	no	no	yes (limited)	only[18]	yes
overlap charges for BC architecture	yes	yes	yes	yes, with extension[22,23]	yes	only[18]	yes
non-quasistatic effects	yes	no	yes	no	yes (limited)	only[17]	yes
fringing effects from layout perspective	no	yes, with extension[21]	yes (limited)	yes, with extension[22,23]	no (limited)	no	yes
linear regime	yes	yes	yes	yes	yes	yes	yes
saturation regime	yes	yes	yes	yes	yes	yes	yes
sub-threshold	yes	yes, with extension[21]	yes	no	yes	only[17,18]	yes
unique formulation for all operation regimes	no	no	yes	no	no	only[17]	yes
charge conservation	yes	yes	no	yes	no	only[9,16,18]	yes
voltage drop at contacts considered	no	yes	yes	no	no	no	yes
references	[7,10]	[11]	[12]	[14]	[15]	[9,16–18]	

If now x is very close to zero, Eq. (2) reduces to:

$$y \approx x. \tag{4}$$

Consequently, for small values, the Lambert W function becomes

$$\mathscr{L}(x) \approx x. \tag{5}$$

With this knowledge, we can simplify the equation for Q'_{ms} for the case of a sub-threshold operation point:

$$Q'_{ms/d,OFF} = \frac{S}{\ln(10)} \cdot C'_{diel} \cdot \exp\left(\frac{V_{gs/d} - V_{T0}}{S/\ln(10)}\right). \tag{6}$$

After this, we continue with the current equation, which for convenience we present here again:

$$I_{ds} = \mu_{eff} \cdot W_{ch} \cdot \left(\frac{k_B \cdot T}{q} \cdot \frac{Q'_{ms} - Q'_{md,barr}}{L_{ch}} + \frac{Q'^2_{ms} - Q'^2_{md,barr}}{2 \cdot L_{ch} \cdot C'_{diel}}\right) \times (1 + \lambda \cdot (V_{ds} - V_{dsx})), \tag{7}$$

Since in the below-threshold regime of operation, the drain Schottky barrier does not have an influence, $Q'_{md,barr} = Q'_{md}$ and hence, we only use Q'_{md}. The current model contains two components: a diffusion component, which consists of the charge densities to the power of one and a drift component, consisting of the charge densities to the power of two. In the sub-threshold regime of operation, the diffusion part dominates over the drift part. The reason is that Q'_{ms} and Q'_{md} are very small in the sub-threshold regime of operation. Thus, the quadrature of Q'_{ms} and Q'_{md} in the drift component results in even smaller values. Due to the dominance of the diffusion current, we can reduce the current equation to

$$I_{ds,OFF} = \mu_{OFF} \cdot \frac{W_{ch,eff}}{L_{ch}} \cdot \frac{k_B \cdot T}{q} \cdot \left(Q'_{ms,OFF} - Q'_{md,OFF}\right), \tag{8}$$

where we omit the channel-length modulation for simplification purposes. In this equation, we can now insert Eqs. (1, 6) which leads to

$$I_{ds,OFF} = \kappa \left(\frac{Q'_{ms,OFF}}{C'_{diel}}\right)^{\beta} \cdot \frac{W_{ch,eff}}{L_{ch}} \cdot \frac{k_B T}{q} \times \left(\frac{S}{\ln(10)} C'_{diel} \cdot \exp\left(\frac{V_{gs} - V_{T0}}{S/\ln(10)}\right) - \frac{S}{\ln(10)} C'_{diel} \cdot \exp\left(\frac{V_{gs} - V_{ds} - V_{T0}}{S/\ln(10)}\right)\right). \tag{9}$$

TABLE S2. Literature summary of organic TFTs with a measured transit frequency of at least 3.5 MHz

reference	f_T [MHz]	μ_{eff} [$cm^2 V^{-1} s^{-1}$]	V_{gs} [V]	V_{T0} [V]	L_{ch} [µm]	$L_{ov,GS}$ [µm]	$L_{ov,GD}$ [µm]	C'_{diel} [$nF cm^{-2}$]	comment
[24]	160	0.62	40	0	1.2	0.21	0.13	8.54	n-channel TFT
[25]	45	1.9	-7	1	1.5	1	1	130	p-channel TFT
[26]	40	n/a	8.6	n/a	0.2	n/a	n/a	n/a	vertical OPBT
[27]	38	4.2	-15	-3	1.5	2	2	36	p-channel TFT
[28]	27.7	2.22	20	9	2	2.5	2.5	29	n-channel TFT
[29]	24	2	-15	0	1.4	2.7	2.7	8	p-channel TFT
[29]	22	1.58	-12	0	1.2	2.3	2.3	8	p-channel TFT
[20]	21	2.7	-3	-1	0.6	1.7	8.3	700	p-channel TFT
[30]	20	1.11	20	8.6	2	1	1	20	n-channel TFT
[31]	20	0.4	-20	0	2.5	0.5	0.5	24	p-channel TFT
[32]	20	0.44	-15	0	0.8	n/a	n/a	23	vertical transistor
[33]	20	0.82	30	0	1.75	3	3	6	n-channel TFT
[34]	20	2.7	-10	-5	3	2.25	2.25	80	p-channel TFT
[35]	19	2.5	-10	0	2	1	3	77	p-channel TFT
[36]	19	1	12	1	1.2	2.3	2.3	27	n-channel TFT
[37]	14.4	0.3	7	0.5	1	1.7	1.7	39	n-channel TFT
[28]	11.4	0.73	-20	-4	2	2.5	2.5	20	p-channel TFT
[38]	10.4	2.2	-3	-0.7	0.85	5	5	700	p-channel TFT
[39]	9.7	n/a	-8.2	-3	0.4	n/a	n/a	50	vertical transistor
[40]	6.7	2	-3	-1.2	0.6	5	5	700	p-channel TFT
[41]	4.9	0.11	30	5	1.8	3	3	10	n-channel TFT
[42]	4.3	0.58	20	5	6	4.5	4.5	27.5	n-channel TFT
[43]	4.1	0.5	-3	-1.2	1	1	9	700	p-channel TFT
[44]	3.7	0.5	-3	-1.2	0.6	5	5	700	p-channel TFT

Now, we insert the equation for $Q'_{ms,OFF}$ in the power-law mobility, which then results in

$$\begin{aligned} I_{ds,OFF} =& \kappa \frac{W_{ch,eff}}{L_{ch}} \cdot \frac{k_B T}{q} \cdot \left(\frac{S}{\ln(10)} \right)^{\beta} \exp\left(\beta \frac{V_{gs}-V_{T0}}{S/\ln(10)} \right) \\ & \times \left(\frac{S}{\ln(10)} C'_{diel} \cdot \exp\left(\frac{V_{gs}-V_{T0}}{S/\ln(10)} \right) \right. \\ & \left. - \frac{S}{\ln(10)} C'_{diel} \cdot \exp\left(\frac{V_{gs}-V_{ds}-V_{T0}}{S/\ln(10)} \right) \right). \end{aligned} \tag{10}$$

After some algebra, we can rearrange this to

$$\begin{aligned} I_{ds,OFF} =& \kappa \frac{W_{ch,eff}}{L_{ch}} \cdot \frac{k_B T}{q} \cdot \left(\frac{S}{\ln(10)} \right)^{\beta+1} \cdot C'_{diel} \\ & \times \exp\left((\beta+1) \frac{V_{gs}-V_{T0}}{S/\ln(10)} \right) \left(1 - \exp\left(\frac{-V_{ds}}{S/\ln(10)} \right) \right). \end{aligned} \tag{11}$$

In the next step, we define a constant C_1 containing all the factors that do not contain V_{gs}:

$$\begin{aligned} C_1 =& \kappa \frac{W_{ch,eff}}{L_{ch}} \cdot \frac{k_B T}{q} \cdot \left(\frac{S}{\ln(10)} \right)^{\beta+1} \cdot C'_{diel} \\ & \times \left(1 - \exp\left(- \frac{V_{ds}}{S/\ln(10)} \right) \right) \end{aligned} \tag{12}$$

which then allows us to write Eq. (12) in an easier form:

$$I_{ds,OFF} = C_1 \cdot \exp\left((\beta+1) \frac{V_{gs}-V_{T0}}{S/\ln(10)} \right). \tag{13}$$

In order to find an expression for the sub-threshold swing that the model exhibits, we now calculate the logarithm to base 10. Again after some algebra and making use of the fact that $\log_{10}(e) = 1/\ln(10)$, we can write:

$$\log_{10}\left(I_{ds,OFF}\right) = \log_{10}(C_1) + (\beta+1) \frac{V_{gs}-V_{T0}}{S}. \tag{14}$$

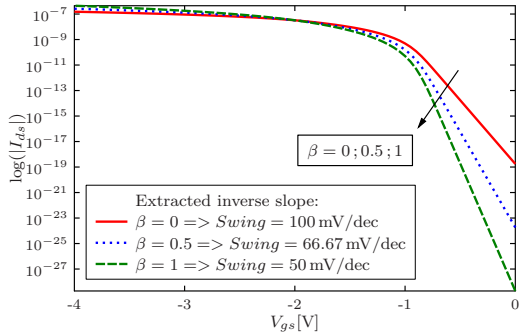
We now derive the current in logarithmic scale and take the inverse value of that, which is in fact the sub-threshold swing that the model exhibits:

$$S_{obs} = \frac{dV_{gs}}{d\log_{10}\left(I_{ds,OFF}\right)} = \frac{S}{(\beta+1)}. \tag{15}$$

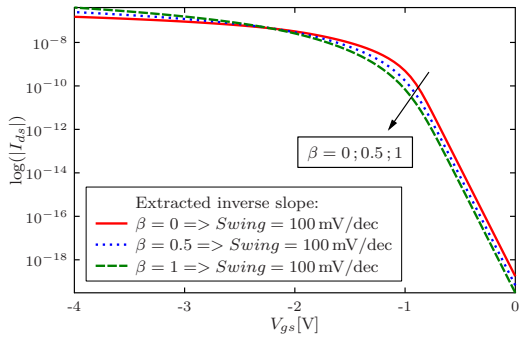
We can see that only for the case that $\beta = 0$, the observable slope S_{obs} is equal to the slope S that is set in the model parameters. Furthermore, this equation allows us to calculate the slope S that we need to set in the model parameters so that the model exhibits the desired S_{obs}:

$$S = S_{obs} \cdot (\beta + 1). \tag{16}$$

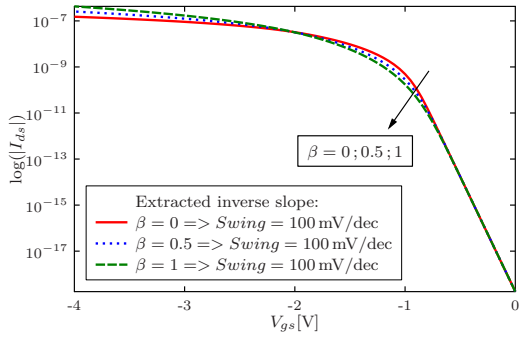
In our compact model, we now use this compensation equation. The observed swing in the IV characteristics is entered in our model parameters and is subsequently multiplied by $(\beta+1)$ and this corrected swing is then used internally. As can be seen in Fig. S1(b), the sub-threshold swing is now constant, even if β is altered. However, another effect becomes visible: Changing the value of β has an effect on the threshold



(a)



(b)



(c)

FIG. S1. (a) Transfer characteristics as calculated by the compact model. The fitting parameters are equal for each transistor except for the power-law mobility exponent. It can be seen that β alters the sub-threshold swing. In the model, a value of $S = 100\,\mathrm{mV/dec}$ is set, but the sub-threshold swing which the model really exhibits changes. The extracted swings are given in the inset. (b) The same characteristics as in (a) are shown, but here, the compensation of the influence of β is performed. (c) Again the same characteristics as in (a) are shown, but here, both compensations are conducted: The sub-threshold swing and the threshold voltage are de-coupled from the influence of β.

voltage, since the curves are shifted along the V_{gs}-axis. Following a similar analysis as for the sub-threshold swing, we can derive an equation for the shift ΔV_{T0} which the threshold voltage exhibits in dependence of β. This leads to the following analytical equation:

$$\Delta V_{T0} = \frac{S_{obs}}{\ln(10)} \cdot \ln\left((\beta+1)^{\beta+1} \cdot \left(\frac{S_{obs}}{\ln(10)} \right)^{\beta} \right), \qquad (17)$$

where S_{obs} is the sub-threshold swing that the model will *really* exhibit (i.e. which is set as model parameter). Incorporating the shift of the threshold voltage and the correction of the swing into the equation for the charge densities per gate area leads to the following equation:

$$Q'_{ms/d} = \frac{(\beta+1)\,S_{obs}}{\ln(10)} C'_{diel} \mathscr{L}\left\{ \exp\left(\frac{V_{gs/d} - V_{T0} + \Delta V_{T0}}{(\beta+1)\,S_{obs}/\ln(10)} \right) \right\}. \qquad (18)$$

In Fig. S1(c), the transfer curves of the same transistor as in the other two sub-figures are shown, but here, the de-coupling of the sub-threshold swing and of the threshold voltage from β are implemented. It can be seen that now, the model behaves as it is expected to.

SHORT-CHANNEL EXTENSION FOR THE QUASISTATIC AC MODEL

Introductory Information

As explained in the manuscript, a correction of the AC model has been performed in order to cope with short-channel transistors. In this section, we will give some more background information about the origin of the fitting function according to Eq. (23) in the manuscript.

In ref.[45], the influences of the Schottky barriers at the source and drain are incorporated into the DC model in different ways. The influence of the source Schottky barrier is included by calculating an equivalent barrier resistance $R_{sb,s}$. According to the same principles as described in ref.[46], this resistance is then included in terms of an effective mobility, thus reducing the current. Theoretically, Eq. (38) in ref.[45] describes the voltage drop $V_{sb,s}$ over the source Schottky barrier. However, this voltage drop may not be regarded as the *true* voltage drop over the source Schottky barrier, because it does not contain any information about the non-linear behavior of the Schottky barrier arising from the effect of Schottky barrier lowering. Rather, this value for $V_{sb,s}$ has to be regarded as an auxiliary value that is used in order to define a resistance $R_{sb,s}$. The difficulty is that in principle, the series connection of a transistor and a Schottky diode at the source contact cannot be solved analytically. A numerical solution, e. g. using the Newton algorithm would be required. Therefore, in ref.[45], the way of calculating $R_{sb,s}$ circumvents this problem, even though it is known that this method uses some approximations. Anyway, by the definition of the fitting parameters η and θ, the behavior of the source Schottky barrier can be captured.

By contrast, the voltage drop $V_{sb,d}$ over the drain Schottky barrier is calculated directly without the definition of an equivalent barrier resistance. The reason for this is that a forward-driven Schottky diode in series with the drain contact of a transistor is easier to treat, since the voltage drop $V_{sb,d}$ only alters the drain-source voltage and does not affect the intrinsic gate-source voltage of the transistor. Additionally, a

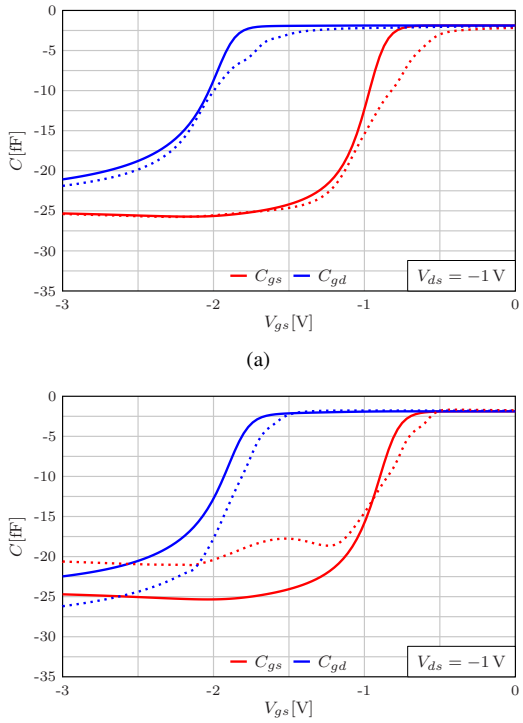


FIG. S2. Quasistatic capacitances C_{gs} and C_{gd} of the compact model (solid lines) in comparison to the results of a TCAD Sentaurus simulation (dotted lines). In both plots, the capacitances are plotted over V_{gs} at a constant drain-source voltage of $V_{ds} = -1\,\mathrm{V}$. (a) Here, the work functions of the source and drain electrodes are aligned with the HOMO of the organic semiconductor. Hence, there is no contact resistance. Even if there are inaccuracies at the transition from the off-state to the on-state, the compact model agrees well with the TCAD simulation. (b) The work functions of the source and drain electrodes are not aligned with the HOMO of the organic semiconductor. There is a workfunction mismatch of 0.49 eV. It can be seen that the compact model fails to reproduce the quasistatic capacitances, especially at high gate-source voltages.

barrier-lowering effect does not appear at the drain Schottky barrier and must not be considered. By contrast, the voltage drop $V_{sb,s}$ over the source Schottky barrier alters both the gate-source voltage and the drain-source voltage. A further important point is the fact that the drain barrier does not affect the drain current in the saturation regime. This enables a calculation of the voltage drop $V_{sb,d}$ in this operation regime by an organic TFT without a drain barrier, which leads to $V_{sbd,sat}$. This generic modeling approach leads to a quite precise expression for the voltage drop $V_{sb,d}$ which makes an implementation into the bias conditions (drain-source voltage) possible, in contrast to the modeling of the source barrier. For a good reproduction of measured and simulated current-voltage characteristics, it was thus sufficient in ref.[45] to model the voltage drop over the drain Schottky barrier as a linear function of the drain-source voltage $V_{sb,d} = f(V_{ds})$ in the linear regime of the IV characteristics of the organic TFT. Here, the linear function begins at $V_{ds} = 0\,\mathrm{V}$, where $V_{sb,d}$ is also 0 V and $V_{sb,d}$ saturates approximately in the saturation regime of the IV characteristics of the transistor to $V_{sb,d} = V_{sb,d,sat}$. Although we know that the drain Schottky diode affects the drain current especially for low drain-source voltages in an exponential way and not linearly, this simplification is legit, since the source diode is much more dominant in this regime.

The simplifications made in the modeling of the Schottky diodes in ref.[45] provide a good model for the current-voltage characteristics, but they do not allow for a precise distinction between the different contact elements. Furthermore, the inclusion of the source Schottky barrier resistance $R_{sb,s}$ in terms of an effective mobility also imposes inaccuracies. Anyway, the combination of the different models and thoughts leads to a comparatively easy, closed-form DC model that shows a good reproduction of measured and simulated current-voltage characteristics.

Derivation of the correction function

As presented in the manuscript, a fitting function f_{fit} and a distribution factor K_r have been defined. We will now explain the observations that led to the the definition of such correction methods. For this purpose, a 2D TCAD Sentaurus[47] simulation of a TC organic TFT has been conducted. A transistor with the following parameters has been simulated: Channel length $L_{ch} = 2\,\mu\mathrm{m}$, channel width $W_{ch} = 1\,\mu\mathrm{m}$, relative dielectric permittivity of the gate dielectric $C'_{diel} = 4.88$, relative dielectric permittivity of the depleted organic semiconductor $C'_{r,osc} = 3$, gate dielectric thickness $t_{diel} = 5.3\,\mathrm{nm}$, organic semiconductor thickness $t_{osc} = 25\,\mathrm{nm}$, and highest occupied molecular orbital energy $E_{HOMO} = 5.19\,\mathrm{eV}$. The work function of the drain/source electrodes was set to $\Phi_{m,SD} = 5.19\,\mathrm{eV}$ for one simulation and to $\Phi_{m,SD} = 4.7\,\mathrm{eV}$ for another simulation in order to create a Schottky barrier between the source/drain contacts and the organic semiconductor. In the Sentaurus TCAD simulation the frequency of the AC analysis was set to a very low value of $f = 0.001\,\mathrm{Hz}$ in order to provide quasistatic results. The quasistatic DC model according to[8] was used for the fitting of the simulation without Schottky barriers and the extension according to[45] was used for the simulation incorporating Schottky barriers. The fittings of the DC model to the different TCAD simulations are not shown here.

In Fig. S2(a), the quasistatic capacitances C_{gs} and C_{gd} of the compact model are compared to the results of the TCAD simulation. Here, no Schottky barrier is present. It can be seen that the compact capacitance model has a good agreement with the simulated curves, except for small deviations around the voltages where the absolute values of the capacitances start to change quickly. If we activate the Schottky barriers in the TCAD simulation, then our model is not capable of reproducing the simulated capacitances. This is shown in Fig. S2(b), where a Schottky barrier of 0.49 eV is

present. As supported by Fig. 4 in the manuscript, there is a notable influence of the source Schottky barrier on the charge density Q'_{ms} at the source end of the channel. At this stage, in the capacitance model we disregard the voltage drops over the Schottky barriers at the source and drain. It is thus obvious why the model fails to reproduce the capacitances.

Next, we evaluate different approaches to include the influence of the Schottky barriers at the source and drain correctly in our model. A first try is to use the voltage drops $V_{sb,s}$ and $V_{sb,d}$ according to ref.[45]. We directly use the voltage drop $V_{sb,s}$ as the contact voltage at the source. As explained in the manuscript, our model also contains an Ohmic contact resistance, which is included in the model by altering the effective mobility, just in the same way as $R_{sb,s}$ is included. We now attribute this voltage drop to belong to the drain side and calculate the drain contact voltage as $V_{d,contact} = V_{sb,d} + |I_{ds}| \cdot R_C$. Then, based on $V_{sb,s}$ and $V_{d,contact}$, we recalculate the charge densities Q'_{ms} and Q'_{md} for the AC model. However, this leads to bad results, as shown in Fig. S3(a). Even though the capacitance C_{gd} shows a somehow acceptable agreement, the capacitance C_{gs} entirely fails. This reveals that we cannot simply take $V_{sb,s}$ according to ref.[45] and it supports the explanation that $V_{sb,s}$ serves more as an auxiliary value that is used to calculate an equivalent barrier resistance, since, as mentioned before, the expression for $V_{sb,s}$ does not include the important influence of the barrier lowering. Furthermore, we may have to rethink where to attribute the Ohmic part R_C of the contact resistance.

The next experiment is to calculate the voltage drop over the source Schottky barrier differently. Since the equivalent resistance $R_{sb,s}$ of the source Schottky barrier, which includes the barrier lowering effect, is known and since the drain-current is also known from the DC model, the voltage drop could be calculated alternatively as $V_{sb,s,alt} = |I_{ds}| \cdot R_{sb,s}$. The voltage drop over the drain contact is kept as in the section before: $V_{d,contact} = V_{sb,d} + |I_{ds}| \cdot R_C$. In Fig. S3(b), the results are shown when this method is applied. It can be seen that now, the compact-modeled C_{gs} shows a rather good agreement, whereas C_{gd} fails. These observations show that additional adjustments are necessary in the AC model, if contact elements are present.

Due to the discrepancies between the TCAD-simulated capacitances and the compact model, the fitting function f_{fit} and the distribution factor K_r are necessary. Since all the further derivation steps would go too much into detail, we only present the final result here. If we use f_{fit} and K_r, we have the possibility to tune the transition of the capacitances from the off-state to the on-state and also the shape of the curves. Figure S3(c) shows the two capacitances again, this time incorporating f_{fit} and K_r. The parameter of the fitting function has been chosen as $K_1 = 0.2$ and the parameter K_r has been chosen as $K_r = 0.15$. Even if the shape of C_{gs} is not perfect in the transition regime from the off-state to the on-state, the overall agreement is quite good now. Furthermore, which is more crucial, the agreement is high for high absolute values of V_{gs}. Since the transistors under investigation in this work are operated at high gate-source voltages, a correct AC model at high gate-source voltages is important. Quasistatic capacitance measurements are not available for the transistors under investigation here, but the parameters K_1 and K_r are used as fitting parameters for the trends of h_{21}.

FITTING OF THE QUASISTATIC DC AND AC MODEL

In this section, the fitting of the quasistatic DC and AC model for the TC and BC transistors is presented. All transistors use a basic parameter set, which is shown in Tab. (S3). The DC fitting of the transistors is then performed by varying a subset of parameters, which is shown in Tab. (S4) for the TC transistors and in Tab. (S5) for the BC transistors. In these tables, the gate-to-contact overlap lengths are the measured values. It has to be pointed out that the BC transistor with $L_{ov,GS} = 6.5\,\mu\text{m}$ is an outlier which has a much lower low-field mobility ($\kappa = 0.7\,\text{cm}^2\text{V}^{-\beta-1}\text{s}^{-1}$). The channel lengths were measured, but in a certain range of $\mp 50\,\text{nm}$, they are regarded as fitting parameters for the current. The parameters of the non-linear injection model are determined by numerically optimizing the model curves so that they agree with the measured data. The initial Schottky barrier height, Φ_{B0}, is theoretically defined by the band diagram (see Fig. 5 in the main document). However, the exact barrier height is not known. Since the Schottky barrier resistance is dependent not only on Φ_{B0}, but also on other fitting parameters, the exact value of Φ_{B0} is not essential for the correct reproduction of the measured DC curves. Since there are no quasistatic capacitance measurements available, we cannot determine the short-channel capacitance fitting parameters K_{fit} and K_r for each transistor. The values of these two parameters are regarded as fitting parameters so that the resulting small-signal gain h_{21} provides a good fitting. The TC transistors have an overlap-length-dependent contact resistance R_{const}. For all TC transistors, a transfer length of $L_t = 1.16\,\mu\text{m}$ and a sheet resistance of $R_{sheet} = 5800\,\Omega$ have been assumed.

The gate leakage current in all the DC measurements is exceedingly low ($\approx 1\,\text{pA}$) and none of the TFTs show noticeable hysteresis. One striking difference between the two architectures is that the off-state drain current is much higher for the TC TFTs than for the BC TFTs. This likely occurs due to short-channel effects which we have covered in detail in previous work[48].

TLM MEASUREMENTS

The transmission line method (TLM) has been used to determine the contact resistance and mobility of the TC transistors. In Fig. S4, the results of the TLM are shown. The transistor is treated as a series connection of a transistor and a contact resistance R_C. By measuring the total resistance of transistors with different channel lengths, the contact resistance can be

TABLE S3. Basic fitting parameters for TC and BC

Parameter	TC	BC
$C'_{diel}[\mathrm{nF\,cm^{-2}}]$	500	500
$\kappa[\mathrm{cm^2 V^{-\beta-1} s^{-1}}]$	1.1	2.1
$\beta[-]$	0.4	0.5
$\lambda[\mathrm{V^{-1}}]$	0.07	0.07
$N_{fing}[-]$	4	4
$W_{fing}[\mu\mathrm{m}]$	25	25
$d_{fing}[\mu\mathrm{m}]$	20	20
$w_{ovl}[\mu\mathrm{m}]$	30	30
$\Phi_{B0}[\mathrm{eV}]$	0.4	0.4
$\eta[-]$	0.9855	1.3047
$\theta[-]$	1.7	1
$d_m[\mathrm{nm}]$	-	5
$d_B[\mathrm{nm}]$	-	3.2187
$K_{sat}[-]$	0.63	1.3
$C_{scale,high}[-]$	0	0
$C_{scale,low}[-]$	1	1
$p_{scale}[-]$	1	50
$\tau_{scale}[\mathrm{s}]$	0.4×10^{-7}	variable
$C_{scale2,high}[-]$	0	0
$C_{scale2,low}[-]$	1	1
$p_{scale2}[-]$	2.5	2.5
$\tau_{scale2}[\mathrm{s}]$	variable	0.5×10^{-7}
$K_{fit}[-]$	0.9	1
$K_r[-]$	variable	0

TABLE S4. Specific fitting parameters for the TC transistors along with the measured gate-to-contact overlap lengths

$L_{ov,GS}$ [µm]	$L_{ov,GD}$ [µm]	L_{ch} [µm]	S_{sth} [mV/dec]	V_{t0} [V]	δ_{fit} [−]	K_r [−]	τ_{scale2} [s]
9.2	1.4	0.69	250	-0.87	0.6	0.07	0.04e-7
8.4	2.4	0.67	240	-0.87	0.6	0.07	0.063e-7
7.4	3.4	0.67	240	-0.88	0.6	0.15	0.08e-7
6.4	4.2	0.66	230	-0.9	0.6	0.27	0.12e-7
5.4	5.2	0.67	230	-0.92	0.6	0.44	0.17e-7
4.5	6.0	0.66	230	-0.92	0.6	0.55	0.2e-7
3.5	7.0	0.66	230	-0.93	0.6	0.7	0.25e-7
1.9	8.5	0.67	230	-1	0.36	0.95	0.3e-7
0.9	9.6	0.68	230	-1	0.26	0.95	0.45e-7

TABLE S5. Specific fitting parameters for the BC transistors along with the measured gate-to-contact overlap lengths

$L_{ov,GS}$ [µm]	$L_{ov,GD}$ [µm]	L_{ch} [µm]	S_{sth} [mV/dec]	V_{t0} [V]	R_{const} [Ω]	δ_{fit} [−]	τ_{scale} [s]
9.4	0.8	0.67	72	-0.69	630	0.65	0.037e-7
8.4	1.9	0.64	71	-0.7	540	0.65	0.04e-7
7.4	3.0	0.66	70	-0.7	580	0.65	0.045e-7
6.5	4.0	0.66	80	-0.67	560	0.65	0.032e-7
5.8	4.7	0.66	71	-0.7	640	0.65	0.055e-7
4.8	5.7	0.66	71	-0.71	590	0.65	0.06e-7
3.6	6.8	0.69	72	-0.7	730	0.45	0.11e-7
2.8	7.6	0.63	71	-0.69	530	0.45	0.11e-7
1.7	8.6	0.63	71	-0.69	470	0.45	0.1e-7
0.8	9.7	0.66	71	-0.68	500	0.3	0.27e-7

separated from the intrinsic channel resistance. The values extracted by the TLM are not necessarily the same values as those which are set in the compact model. The reason for this is that in the compact model different effects are included, such as the current spreading, the splitting-up of contact resistances into Ohmic and Non-Ohmic components, etc. Thus, we can say that the transmission line consisting of the transistor and the contact resistances conducts the same current as measured.

VECTOR NETWORK ANALYZER

The small-signal gain h_{21} is determined based on measurements of the scattering parameters (S-parameters) of the transistors. Standard conversions according to[49] allow to convert the measured S-parameters to the small-signal gain h_{21}. When observing the small-signal gain according to Fig. 10 in the main document, one effect becomes visible: For low frequencies, the measured h_{21} forms a plateau, which is more pronounced for the TC transistors than for the BC transistors. We can reasonably attribute this behavior to the measurement system and not to a physical effect in the transistors for the following reasons: while gate-to-contact leakage currents can degrade this slope, the leakage currents in the transistors are found to be so low ($< 1\,\mathrm{pA}$) that this cannot justify the observed drop in h_{21} at low frequencies. In addition, the admittances between the gate contact and the other contacts become extremely low ($\approx 30\,\mu\mathrm{S}$), which brings the measurement system close to its resolution limit. Therefore, meaningful evaluation of the AC performance of the TFTs is only performed for the higher frequency regions starting where $^{d|h_{21}|}/_{d\log(f)} \approx -20\,\mathrm{dB/dec}$.

MIM VS. MISM

In our discussion in the main document, we pointed out that the capacitance C_{gs} is very similar for both transistor architectures (TC and BC) in the chosen operation point of $V_{gs} = V_{ds} = -3\,\mathrm{V}$.

By contrast, C_{gd} varies substantially between both architectures. We will now show the results of a TCAD Sentaurus simulation proving our assumptions. The gate-to-contact overlap region of a BC transistor is in principle a metal-insulator-metal (MIM) structure, where next to this stack an un-patterned region of organic semiconductor is present, which is denoted as a fringe region. Such a structure is depicted in Fig. S5(a). The gate-to-contact overlap region of a TC transistor is very similar to this structure, but the difference is that the golden S/D electrode is separated from the gate dielectric by an intervening layer of organic semiconductor. This results in a metal-insulator-semiconductor-metal (MISM) structure, where as well un-patterned fringe regions of OSC are found next to the stack. Figure S5(b) depicts such a structure. We can distinguish between two different operation regimes of these structures:

- Depletion: The absolute value of the voltage is low so that the organic semiconductor is depleted. The MIM structure behaves like a plate capacitance and the only capacitance which can be measured is the gate dielectric capacitance C'_{diel}. The MISM structure behaves like a series connection of two capacitances: the gate dielectric capacitance and the dielectric capacitance of the depleted organic semiconductor. If the dimensions of a MIM and a MISM structure are equivalent, we can expect that the MIM structure will exhibit a higher absolute capacitance, which can be proven by observing Fig. S5(c) for low absolute values of the voltage.

- Accumulation: The absolute value of the voltage is high so that the organic semiconductor is driven into accumulation. According to the theory[8], the density of quasi-mobile accumulation charges in direct proximity to the insulator is given by $Q'_m = C'_{diel}(V - V_{T0})$, where V_{T0} is the threshold voltage. This is valid in the whole plane where the organic semiconductor touches the gate dielectric. Obviously, the density of accumulated charges is proportional to the gate dielectric capacitance, just as the geometric plate capacitance of a MIM structure. A further and important aspect is that due to the exponential increase of accumulation charges with increasing electrostatic potential, the electrostatic potential in the semiconductor close to the gate insulator only exhibits minor changes when the voltage between the contacts is further increased. As a consequence, in MISM structures the voltage drop over the series connection of the gate dielectric capacitance and the capacitance of the depleted organic semiconductor is nearly constant above the threshold. This means that in a MISM structure, the dominant capacitance in accumulation is the capacitance due to the accumulation charges Q'_m. The interesting consequence from these theoretical thoughts is that a MIM structure and a MISM structure converge to exactly the same capacitance when operated in high accumulation. This is proven by the TCAD Sentaurus simulation results shown in Fig. 5(c).

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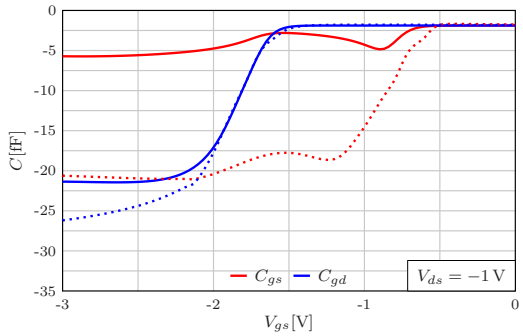
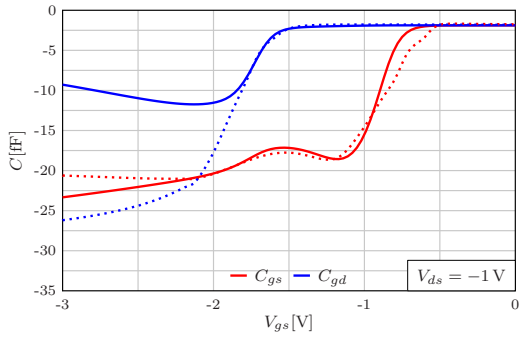
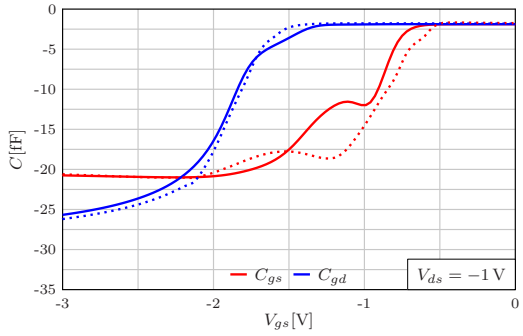


(a)

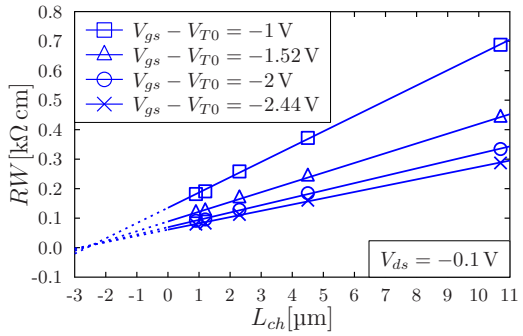


(b)

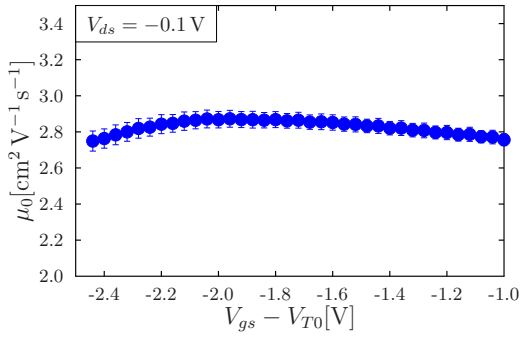


(c)

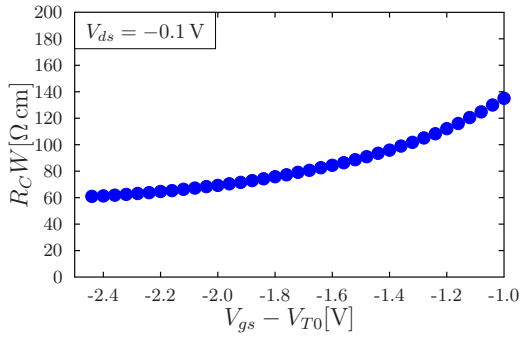
FIG. S3. Quasistatic capacitances C_{gs} and C_{gd} of the compact model (solid lines) in comparison to the results of a TCAD Sentaurus simulation (dotted lines). In all plots, the capacitances are plotted over V_{gs} at a constant drain-source voltage of $V_{ds} = -1\,\mathrm{V}$. A work function mismatch of 0.49 eV between the source/drain electrodes and the organic semiconductor is present. (a) In the compact model, the original, non-modified voltage drops $V_{sb,s}$ and $V_{sb,d}$ over the source/drain Schottky barriers are taken as defined in[45]. Whereas the capacitance C_{gd} has an adequate agreement, the capacitance C_{gs} fails. (b) Instead of the voltage drop $V_{sb,s}$ over the source Schottky barrier according to[45], the source voltage drop is calculated as follows: $V_{sb,s} = |I_{ds}| \cdot R_{sb}$. The voltage drop $V_{sb,d}$ over the drain Schottky barrier is the same as in (a). Now, C_{gs} has a better agreement, but C_{gd} fails. (c) Here, the new model incorporating f_{fit} and the distribution factor K_r is used. Although the model has some deviations in the transition regime between off-state and on-state, the overall fitting is good now, especially for high gate-source voltages.



(a)



(b)



(c)

FIG. S4. (a) Measured width-normalized resistance of the series connection of a transistor and a contact resistance vs. channel length for different overdrive voltages $V_{gs} - V_{T0}$. The measured points are connected by linear regression functions. The linear regression functions are extrapolated and their intersection with the RW-axis yields the contact resistance $R_C W$. The measurements were conducted at $V_{ds} = -0.1\,\mathrm{V}$. (b) Mobility μ_0 as extracted by the TLM vs. overdrive voltage. (c) Width-normalized contact resistance as extracted by the TLM.

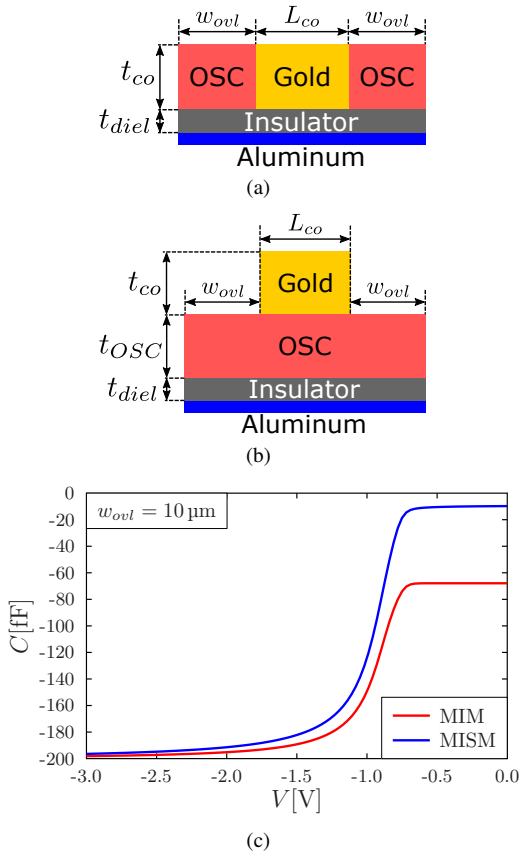


FIG. S5. (a) Sketch of a metal-insulator-metal (MIM) structure including fringing regions. An equivalent structure is found in BC transistors in a cutplane in the source/drain regions. (b) Sketch of a metal-insulator-semiconductor-metal (MISM) structure including fringing regions. An equivalent structure is found in TC transistors in a cutplane in the source/drain regions. (c) Quasistatic capacitance-voltage characteristics of the MIM and MISM structures as a result of a TCAD Sentaurus simulation. The dimensions are: $L_{co} = 10\,\mu m$, $w_{ovl} = 10\,\mu m$, $t_{co} = 40\,nm$, $t_{diel} = 5.3\,nm$, $t_{OSC} = 25\,nm$. In depletion, bot structures show different capacitances, but in accumulation, both converge to the same value, as predicted.