Modeling the Short-Channel Effects in Coplanar Organic Thin-Film Transistors

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***Abstract*— We have developed models for three different short-channel effects [subthreshold-swing degradation, threshold-voltage roll-off, and drain-induced barrier lowering (DIBL)] in coplanar organic thin-film transistors (TFTs) and verified them against the measured current–voltage characteristics of TFTs having channel lengths as small as 0.5 μm. To derive the models, the Schwarz–Christoffel transformation was applied to obtain a complex mapping function that links the coplanar device geometry to an equivalent geometry in a different coordinate system in order to solve Laplace's equation of the 2-D potential problem. The solution to this potential problem serves as the basis for the definition of the short-channel models, which can be incorporated into any compact dc models for coplanar TFTs that use the TFTs' threshold voltage and subthreshold swing as input parameters. To verify the model, the channel-length-dependent effects were extracted from technology computer-aided design (TCAD) simulations (transfer characteristics and surface-potential profile) and from measurements performed on organic p-channel TFTs fabricated using high-resolution stencil lithography.**

***Index Terms*— Coplanar device architecture, drain-induced barrier lowering (DIBL), modeling, organic thin-film transistors (TFTs), short-channel effects, threshold-voltage shift.**

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I. Introduction

THE design of integrated circuits and systems based on organic thin-film transistors (TFTs) requires accurate device compact models to support time-efficient and meaningful circuit simulations [1], [2]. The compact models must capture all relevant intrinsic and extrinsic device effects, including those that occur upon aggressive reductions of the channel length [3], which are required for improving the dynamic TFT and circuit performance [4]–[7]. These short-channel effects include the degradation of the subthreshold swing, the threshold-voltage roll-off, and the drain-induced barrier lowering (DIBL) effect, all of which are known from silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) [8], [9]. Physics-based models for these short-channel effects have been reported for organic TFTs fabricated in the staggered device architecture [14], but not for organic TFTs in the coplanar architecture.

In this article, a potential solution for the coplanar TFT architecture is derived in order to define analytical and physics-based model equations for subthreshold-swing degradation, threshold-voltage roll-off, and DIBL that are suitable for implementation in compact dc models of such TFTs, with an emphasis on submicro channel-length devices [10]–[13]. The models include empirical approaches to compensate the subthreshold swing degradation due to traps. The general scheme and the steps of defining the potential problem, of performing the conformal mapping, of adapting an existing potential, and of defining the model are all very similar to the model derivation outlined in [14]. For detailed explanations of some of the techniques and methods utilized here, the reader is thus referred to [14].

In Section II, the potential solution in [14] is summarized, and its adaptation to the coplanar device architecture is explained. In Section III, the results produced by the short-channel models are fit to measurement data obtained from coplanar organic TFTs with channel lengths between 0.5 to 10 μm and to the results of technology computer-aided design (TCAD) simulations of TFTs with channel lengths down to 0.1 μm. In Section IV, the newly developed short-channel models are incorporated into the compact dc model that was reported in [16], and the resulting improvement of the current model is illustrated by the successful fitting to the measured current–voltage characteristics of the TFTs.

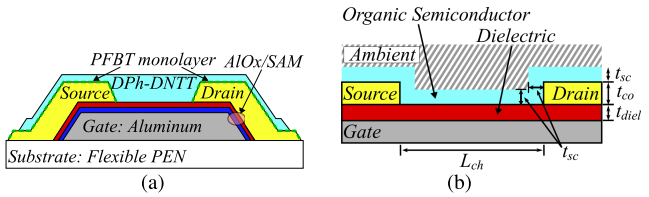

Fig. 1. (a) Schematic cross section and (b) simplified geometry of the coplanar organic TFTs considered in this work, where t_{diel} is the thickness of the gate dielectric, t_{sc} is the thickness of the semiconductor layer, t_{co} is the thickness of the contacts, and L_{ch} is the channel length.

II. Surface Potential

In this section, the fundamentals of the approach reported in [14] pertaining to staggered TFTs are summarized, and the modifications required for calculating the surface potential of coplanar TFTs are introduced.

A. Definition of the Potential Problem

The expressions for the flatband voltage V_{fb} and the built-in voltage V_{bi} at the source and drain contacts depend on the difference between the work functions of the source/drain or gate metal ($\Phi_{m,s/d}$ and $\Phi_{m,g}$) and the work function of the semiconductor

$$V_{\text{bi}} = \Phi_{m,s/d} - \left(\chi_{\text{sc}} + \frac{E_g}{2q}\right) \tag{1}$$

$$V_{\text{fb}} = \Phi_{m,g} - \left(\chi_{\text{sc}} + \frac{E_g}{2q}\right) \tag{2}$$

where q is the elementary charge, χ_{sc} is the electron affinity of the semiconductor, and E_g is the difference between the energy of the lowest unoccupied molecular orbital (LUMO) and the energy of the highest occupied molecular orbital (HOMO) of the organic semiconductor. These parameters are incorporated in the boundary conditions for the source, drain, and gate contacts

$$\Phi_s = V_s - V_{\text{bi}} \tag{3}$$

$$\Phi_d = V_d - V_{\text{bi}} \tag{4}$$

$$\Phi_g = V_g - V_{\text{fb}}. \tag{5}$$

To allow the potential problem to be solved, the geometry in Fig. 1(b) is simplified to the geometry in Fig. 2. Here, the ambient region in Fig. 1(b) is ignored, and the contact-to-gate overlap lengths are assumed to be infinite. The thickness of the semiconductor (t_{sc}) between the inner edges of the source and drain contacts (i.e., in the channel region) is also assumed to be infinite. The vertical edges of the semiconductor region are defined as the boundaries of the potential problem. The lateral source/semiconductor and drain/semiconductor interfaces (located outside of the channel region) are thus ignored, and the electric field lines at these interfaces are disregarded. The boundaries along the vertical edges of the semiconductor region above the contacts (dashed boundaries in Fig. 2) are modeled in Section II-C as the Neumann boundary (normal vector of the electric field $\vec{E}_n = 0$).

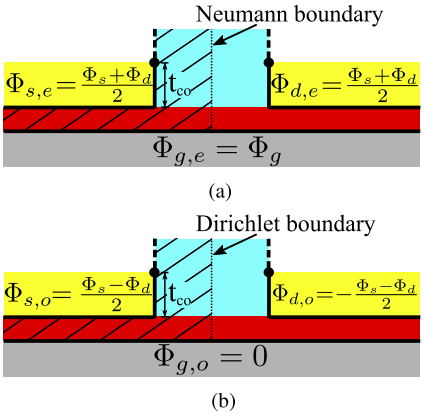

Fig. 2. Decomposition of the original boundary conditions with the contact thickness t_{co} leading to the separated (a) even-mode and (b) odd-mode potential problems.

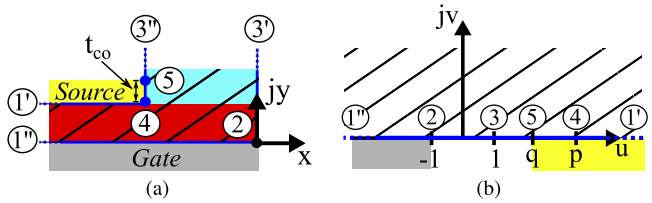

Fig. 3. Source half of the coplanar transistor is mapped from the z-plane into the corresponding geometry in the w-plane in which a specific potential exists that can be used to calculate the potential of the z-plane. The points 3′ and 3″ from the z-plane collapse into a single point 3 in the w-plane. (a) z-plane. (b) w-plane.

Subsequently, the simplified geometry is decomposed into two separate problems [15], namely an even mode and an odd mode, the superposition of which yields the actual potential problem. Fig. 2 shows that both modes have the same geometry, but different boundary conditions that are based on the original boundary conditions Φ_s, Φ_d, and Φ_g. This decomposition leads to a Neumann or Dirichlet boundary along the axis of symmetry in case of the even and the odd mode, respectively. Thus, the potential problem can be reduced to one-half of the transistor for both modes, which is a prerequisite for being able to derive an analytical potential solution.

B. Conformal Mapping Function

The Schwarz–Christoffel transformation is applied to obtain a specific complex conformal mapping function $z = x + jy = f(w)$ of one half of the coplanar geometry, as illustrated in Fig. 3(a). If the potential solution of the problem in the w-plane in Fig. 3(b) is known, the potential in the z-plane can thus be calculated with the help of this mapping function, since the Laplace equation and the Poisson equation are invariant to the transformation from the w-plane to the z-plane [17]. By applying the mapping function, a closed polygon that defines the area of interest (hatched region) and the boundaries in the z-plane is mapped into the w-plane, where the boundaries are located on the horizontal axis and the area of interest is above it. Since the semiconductor and the gate dielectric generally have different permittivities (ε_{sc} and $\varepsilon_{\text{diel}}$), the gate-dielectric thickness t_{diel} is adjusted (as described in [18]) in

order to achieve a homogenous area of interest

$$\tilde{t}_{\mathrm{diel}} = t_{\mathrm{diel}}\varepsilon_{\mathrm{sc}}/\varepsilon_{\mathrm{diel}}. \tag{6}$$

The mathematical complexity of the mapping function depends on the number of vertices that are characterized by a relative change in the angle [vertices 2 and 4 in Fig. 3(a)]. The shape of the geometry is identical to the one defined in [14], so the derivative of the mapping function is given as

$$\frac{dz}{dw} = C\frac{\sqrt{w-p}}{\sqrt{w+1}(w-1)} \tag{7}$$

with

$$p = 1 + \frac{L_{\mathrm{ch}}^2}{2\pi^2 C^2} \tag{8}$$

where L_{ch} is the channel length and C is a coefficient of the general mapping function that is different from the one in [14]. It is calculated with the help of point 1 in Fig. 3 that fulfills the condition of being located at an infinitely large distance from the origin of the coordinate system [17]

$$z_1'' - z_1' = j\pi C \quad \text{leads to} \quad C = -\frac{\tilde{t}_{\mathrm{diel}}}{\pi}. \tag{9}$$

Unfortunately, it is not possible to calculate the location of point 5 in the w-plane ($q = f(t_{\mathrm{co}})$) analytically, since there is no inverse function of the form $w = f^{-1}(z)$ [14]. However, a solution for q is required, since it depends on the contact thickness $q = f(t_{\mathrm{co}})$ and hence, it defines the start/end of the source contact. According to Fig. 3, the range of meaningful values for q can be defined as $1 < q < p$, which corresponds to the range from point 3 to point 4. Thus, q can be modeled with a fitting parameter q_{co} as

$$q = p - q_{\mathrm{co}}(p-1). \tag{10}$$

Here, q_{co} is limited to values between 0 ($t_{\mathrm{co}} = 0$) and 1 ($t_{\mathrm{co}} = \infty$), which captures all realistic values of t_{co}.

Equations (7)–(9) yield the complex mapping function. In Section II-C, a potential solution for the geometry in the w-plane is derived in order to solve the potential problems for the even and the odd mode in Fig. 2.

C. Surface Potential

In [14], a potential solution of the Laplace equation of a geometry consisting of two electrodes Φ_1 and Φ_2 located on the horizontal axis separated by a gap of $2a$ (see Fig. 4) was adapted to solve potential problems similar to the problem introduced here involving the even and odd modes in the w-plane [see Fig. 3(b)]. The electrodes Φ_1 and Φ_2 can be defined as the source contact and the gate electrode of the respective mode, and the gap $2a$ is equal to the distance between the source contact and the gate electrode.

The corresponding complex potential solution of the general problem in Fig. 4 is given by [17]

$$P = \Phi + j\Xi = -\frac{j}{\pi}(\Phi_2 - \Phi_1)\cosh^{-1}\left(\frac{w}{a}\right) + \Phi_1. \tag{11}$$

In order to derive potential solutions for the even and the odd mode in Fig. 2, the location of the source contact and the gate electrode must be defined. In both modes, the

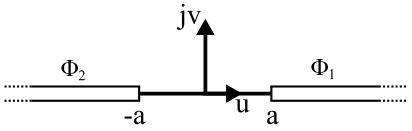

Fig. 4. Geometry whose boundaries are located on the horizontal axis, which consists of two electrodes having a thickness of zero and being separated by a gap of $2a$ [14], [17].

source contact is located between point $1'$ ($u = \infty$) and point 5 ($u = q$) (see Fig. 3), and in the even mode, the gate electrode is defined between point $1''$ ($u = -\infty$) and point 2 ($u = -1$). The gap between the source contact and the gate electrode thus starts at point 2 ($u = -1$) and ends at point 5 ($u = q$). The particular potential solution P_e of the even mode in the w-plane can be obtained by shifting the origin of the coordinate system halfway between both points and determining the value of the parameter a from the distance between them. For this, the variables w and a in (11) must be substituted by

$$w_e = w - \frac{q-1}{2}, \quad a_e = \frac{q+1}{2}. \tag{12}$$

The odd mode, on the other hand, has identical boundary conditions for the gate electrode and the axis of symmetry, which means that these can be combined into an extended gate electrode between the points $1''$ ($u = -\infty$) and $3'$ ($u = 1$). Here, the gap is located between point $3''$ ($u = 1$) and point 5 ($u = q$). In the same way, the particular potential solution for the odd mode P_o is obtained by replacing w and a in (11) by

$$w_o = w - \left(1 + \frac{q-1}{2}\right), \quad a_o = \frac{q-1}{2}. \tag{13}$$

Finally, the particular potential solutions of the even and odd modes P_e and P_o can be used to calculate the potential of a point $P_0(u, v)$ in the w-plane within the region of interest, and with the help of the mapping function, the corresponding point $P_0(x, y)$ in the z-plane can be determined. Superposing both solutions yields the solution of the original potential problem.

However, the explicit calculation of the surface potential in the z-plane would require the inverse function $w = f^{-1}(z)$ of the complex mapping function, which cannot be obtained in closed form. Therefore, as outlined in [14], the function of the potential through the gate dielectric is assumed to be linear in order to be able to calculate the voltage drop across the gate dielectric from the perpendicular electric field along the gate electrode. This perpendicular electric field is obtained in the w-plane by the differentiation of the particular potential solution for both modes (see (11); P_e and P_o). Subsequently, the electric field must be transformed from the w-plane into the z-plane by multiplying with the factor $|dw/dz|$ [17]. Finally, the electric field in the z-plane along the gate electrode can be calculated as follows:

$$\begin{aligned} E_z(w) &= \left|\frac{dw}{dz}\right|\left|\frac{dP_e}{dw}\right| + \left|\frac{dw}{dz}\right|\left|\frac{dP_o}{dw}\right| \\ &= -\left(\Phi_{g,e} - \Phi_{s,e}\right)\frac{(w-1)}{\tilde{t}_{\mathrm{diel}}\sqrt{w-p}\sqrt{w-q}} \\ &\quad -\left(\Phi_{g,o} - \Phi_{s,o}\right)\frac{\sqrt{w+1}(w-1)}{\tilde{t}_{\mathrm{diel}}\sqrt{w-p}\sqrt{w-1}\sqrt{w-q}}. \end{aligned} \tag{14}$$

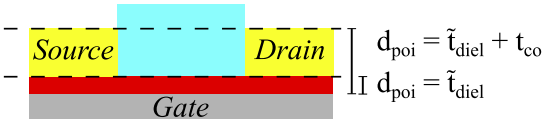

Fig. 5. Schematic cross section of a coplanar TFT. The cutlines along which the potential Φ_{surf} is calculated for $d_{poi} = \tilde{t}_{diel}$ and $d_{poi} = \tilde{t}_{diel} + t_{co}$ are shown as dashed lines.

Since the boundaries of the region of interest are located on the u-axis, the imaginary part v is zero, and finally, the surface potential can be calculated with the help of the boundary condition for the gate electrode as follows:

$$\Phi_{surf}(u) = \Phi_g - E_z(u)\, d_{poi} \tag{15}$$

where d_{poi} is a fitting parameter that defines the distance between the point of interest and the gate electrode. Fig. 5 illustrates the locations of the potential cutlines of Φ_{surf} at $d_{poi} = \tilde{t}_{diel}$ and $d_{poi} = \tilde{t}_{diel} + t_{co}$. To calculate the surface potential, the fitting parameter is set to $d_{poi} = \tilde{t}_{diel}$. By replacing the boundary conditions of the source contact $\Phi_{s,e}$ and $\Phi_{s,o}$ in (14) by the conditions for the drain contact $\Phi_{d,e}$ and $\Phi_{d,o}$ from Fig. 2, the other half of the transistor can be calculated.

III. Model Definition and Verification

The surface potential derived in Section II will now be applied to derive expressions for the subthreshold-swing degradation, the threshold voltage roll-off, and the DIBL. Verification of the model will be performed using the measured current–voltage characteristics of organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) device architecture with channel lengths ranging from 0.5 to 10 μm, and using results of TCAD simulations of coplanar TFTs with channel lengths ranging from 0.1 to 10 μm.

The TFTs were fabricated on flexible polyethylene naphthalate (PEN) substrates by stencil lithography using high-resolution silicon stencil masks [3], [6], [19]. The gate electrode is vacuum-deposited aluminum, and the gate dielectric consists of plasma-grown aluminum oxide and an alkylphosphonic acid self-assembled monolayer with a total thickness of $t_{diel} = 9$ nm. The source and drain contacts are vacuum-deposited gold with a thickness of $t_{co} = 30$ nm, and they are functionalized with a monolayer of pentafluorobenzenethiol (PFBT) to improve the charge injection [20]. The semiconductor is vacuum-deposited dinaphtho[2,3-b:2′, 3′-f]thieno[3,2-b]thiophene (DNTT) with a nominal thickness of $t_{sc} = 20$ nm that varies greatly, due to the pronounced morphology of vacuum-deposited DNTT films [20].

For the simulation model, the following parameters were chosen to simulate the coplanar organic TFTs: thickness of the gate dielectric $t_{diel} = 9$ nm, relative permittivity of the gate dielectric $\epsilon_{r,diel} = 8$, thickness of the organic semiconductor layer $t_{sc} = 25$ nm, relative permittivity of the organic semiconductor $\epsilon_{r,sc} = 3$, thickness of the source and drain contacts $t_{co} = 25$ nm, work function of the gate electrode $\Phi_{m,g} = 4.1$ V, work function of the source and drain contacts $\Phi_{m,s/d} = 5.19$ V, electron affinity of the organic semiconductor $\chi_{sc} = 1.81$ V, HOMO–LUMO energy gap of the organic semiconductor $E_{g,sc} = 3.38$ eV. For the organic semiconductor, a Gaussian density-of-states (DOS) model with the following parameters was assumed: density of states $N_{dos} = 1 \times 10^{21}$ cm^{-3}, standard deviation $\sigma = 0.1$ eV and a shift of the maximum position $E_0 = 0.1$ eV. The charge-carrier mobility in the organic semiconductor of 3 cm^2/(Vs) is assumed to be constant within the semiconductor layer.

A. Subthreshold-Swing Degradation

The subthreshold swing of an ideal long-channel TFT is limited by thermionic emission and is calculated at room temperature ($T = 300$ K) as

$$S = \alpha_{sc}\frac{kT}{q}\ln(10) \approx 60\,\frac{\text{mV}}{\text{dec}} \quad \text{with} \quad \alpha_{sc} = \frac{dV_{gs}}{d\Phi_{surf}(u_{mbh})} = 1 \tag{16}$$

where k is the Boltzmann's constant and u_{mbh} is the maximum-barrier-height position along the gate-dielectric/semiconductor interface in the w-plane. The parameter α_{sc} is defined as the derivative of the gate–source voltage V_{gs} with respect to the surface potential at the position u_{mbh}.

If the channel length is small (in the case of organic TFTs, smaller than 1 μm), the sensitivity of the surface potential with respect to changes in the applied gate–source voltage is reduced by the electrostatic influence of the source and drain contacts acting on the lateral potential profile inside the semiconductor layer. As a result, α_{sc} increases to values greater than unity. The subthreshold swing is extracted at $V_{ds} = 0$ V, and the potential is thus extracted in the center of the channel at $u = -1$. The channel-length-dependent degradation of the subthreshold swing is derived from Φ_{surf} for an operation point of $V_{gs} = V_{fb}$ with a change of dV_g for V_{gs}

$$S_{sc} = \frac{kT}{q}\cdot\frac{\ln(10)}{1 - \dfrac{2\,d_{poi}}{\tilde{t}_{diel}\sqrt{2+\frac{L_{ch}^2}{2\tilde{t}_{diel}^2}}\sqrt{2+\frac{L_{ch}^2}{2\tilde{t}_{diel}^2}}(1-q_{co})}} \tag{17}$$

where $\tilde{t}_{diel}$ is the stretched gate-dielectric thickness defined in (6).

Fig. 6 illustrates the degradation of the subthreshold swing with decreasing channel length calculated using the model presented here (see (17); black line), extracted from the measured transfer characteristics (green triangles), and obtained by fitting the compact dc model presented in [16] individually to the measured transfer curve of each TFT (red circles). The best agreement between the model and the measurements was obtained for $d_{poi} = \tilde{t}_{diel} + 255$ nm and $q_{co} = 0.999$. Also shown in Fig. 6 are results of TCAD simulations of the transfer characteristics (blue circles) and of the surface potential (blue dotted line); in this case, the best agreement with the model (blue line) was obtained for $\tilde{t}_{diel} + 25$ nm and $q_{co} = 0.98$. For all extraction methods, the values of the subthreshold swing (S_{sc}) were normalized to the subthreshold swing of the long-channel TFTs (S_{lc}; $L_{ch} = 10$ μm), which has a value of 69 mV/dec for the measurements, 79 mV/dec for the dc model, and 60 mV/dec for the TCAD simulations. The degradation of the subthreshold swing calculated from the TCAD simulations can be attributed entirely to the influence of the TFT dimensions, since no additional physical models,

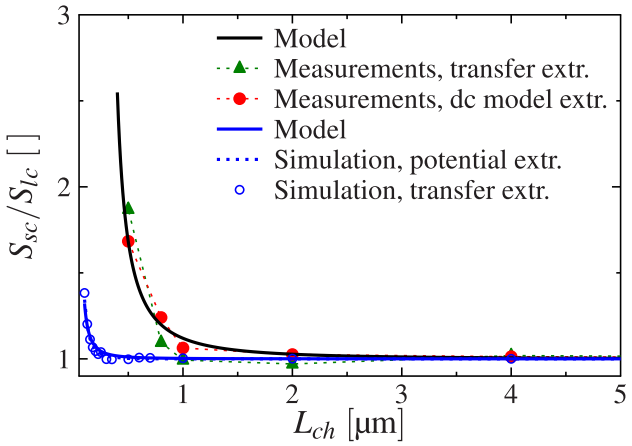

Fig. 6. Degradation of the subthreshold swing with decreasing channel length for organic TFTs with channel lengths ranging from 5 to 0.5 μm, calculated using the model presented here (see (17); black line), extracted from the measured transfer characteristics (green triangles) and obtained by fitting the compact dc model presented in [16] individually to the transfer curve of each TFT (red circles). The best agreement between the model and the measurements was obtained for $d_{poi} = \tilde{t}_{diel} + 255$ nm and $q_{co} = 0.999$. Also shown are results of TCAD simulations of the transfer characteristics (blue circles) and of the surface potential (blue dotted line) for channel lengths ranging from 5 to 0.1 μm; in this case, the best agreement with the model (blue line) was obtained for $d_{poi} = \tilde{t}_{diel} + 25$ nm and $q_{co} = 0.98$.

such as traps within the HOMO-LUMO energy gap, were activated during the simulation. This value of the contact-thickness fitting parameter in the w-plane ($q_{co} = 0.999$) would correspond to a contact thickness (t_{co}) of 65 nm, which is larger than the actual contact thickness (30 nm) by a factor of approximately 2. This discrepancy is due to the fact that (17) ignores the contribution of the electric field lines on the top surface of the source and drain contacts during the definition of the simplified potential problem (see Fig. 3). Since in the subthreshold regime no accumulation channel exists, the leakage current is not expected to flow along the gate-dielectric/semiconductor interface but mostly along the semiconductor/ambient interface, and thus the point of interest should be close to $d_{poi} \approx \tilde{t}_{diel} + t_{sc}$. Equation (17) can be fit successfully to both the measurement results (green triangles) and the compact dc model in [16] (red circles), but the best agreement was obtained for $d_{poi} = \tilde{t}_{diel} + 255$ nm, which is substantially larger than the expected value ($d_{poi} = \tilde{t}_{diel} + 20$ nm). One explanation for the observed increase in the subthreshold swing with decreasing channel length is that in coplanar organic TFTs, the organic-semiconductor morphology is disturbed near the contacts as a result of the contact topography and the surface-energy difference. Trap states arising from the disturbed semiconductor morphology are located near the contacts [21], but for small channel lengths, these trap states may affect a significant portion of the channel area and thus cause a degradation in subthreshold swing. The relative influence of the density per energy (N_t') and energy of these trap states on α, and thus the subthreshold swing, can be written as [16]

$$\alpha_{\text{Traps}} = 1 + \frac{q^2 N_t'}{C_{\text{diel}}'} \tag{18}$$

where C_{diel}' is the unit-area gate-dielectric capacitance. In general, N_t' is assumed to be independent of the channel length. Alternatively, the relation between the subthreshold swing and the trap density can be written as [14]

$$S_{\text{total}} = \alpha_{\text{sc}} \alpha_{\text{Traps}} \frac{kT}{q} \ln(10). \tag{19}$$

When the point of interest in (17) is assumed to be as expected based on the device-fabrication parameters ($d_{poi} = \tilde{t}_{diel} + 20$ nm), (19) can be fit to the measured channel-length dependence of the subthreshold swing (green triangles in Fig. 6) by adapting the value of the trap density N_t' individually for each channel length. This produces values for the trap density ranging from 5.4×10^{12} cm^2 for a channel length of 10 μm to 2×10^{13} cm^2 for a channel length of 0.5 μm. Despite the simplified trap distribution of this model, the values are in the order of magnitude as expected for organic-semiconductor molecules [22]. The relative increase in trap density with decreasing channel length observed here is possibly due to the disturbed semiconductor morphology near the contacts. Nevertheless, it is possible to fit the short-channel model in (17) to the measured subthreshold-swing degradation simply by increasing the value of the point of interest d_{poi}, even if the subthreshold swing is partly degraded by trap states.

B. Threshold-Voltage Roll-Off

The maximum height of the surface potential in the channel region between the source and drain contacts defines the potential barrier that must be lowered by the applied gate field in order to induce a charge-carrier channel in the semiconductor. If the channel length is large, the potential barrier is relatively flat in the channel center, and its height is unaffected by the presence of the source and drain contacts. If, however, the channel length is sufficiently small so that the influence of the source and drain contacts extends to the center of the channel, then the absolute amount of the maximum barrier height is lowered by the influence of the source and drain contacts. This effect can be modeled as a threshold-voltage shift calculated at Φ_{surf} ($u_{\text{mbh}} = -1$) under flatband conditions ($V_{\text{gs}} = V_{\text{fb}}$) for $V_{\text{ds}} = 0$ V, as outlined in [14]

$$\begin{aligned} \Delta V_{T,\text{roll-off}} &= \Phi_{\text{surf,long-ch}}(-1) - \Phi_{\text{surf,short-ch}}(-1) \\ &= V_{\text{bi}} \frac{2\, d_{\text{poi}}}{\tilde{t}_{\text{diel}} \sqrt{2 + \frac{L_{\text{ch}}^2}{2\tilde{t}_{\text{diel}}^2}} \sqrt{2 + \frac{L_{\text{ch}}^2}{2\tilde{t}_{\text{diel}}^2}(1 - q_{\text{co}})}} \end{aligned} \tag{20}$$

where $\Phi_{\text{surf,short-ch}}$ is given by (15) for the case of the short-channel transistor having a channel length L_{ch}.

Fig. 7 illustrates the magnitude of the threshold-voltage shift caused by the roll-off effect with decreasing channel length calculated using (20); (black line), extracted from the measured transfer characteristics (green triangles), and obtained by fitting the compact dc model presented in [16] individually to the measured transfer curve of each TFT (red circles). The best agreement between the model and the measurements was obtained for $d_{poi} = \tilde{t}_{diel} + 11.9$ nm and $q_{co} = 0.999$. Also shown in Fig. 7 are results of TCAD

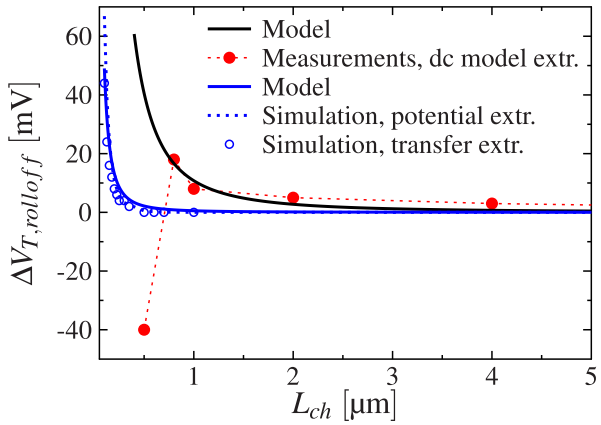

Fig. 7. Threshold-voltage roll-off upon reducing the channel length from 5 to 0.5 μm, calculated using (20) (black line) and compared to the values extracted from the measured transfer characteristics of organic TFTs having channel lengths ranging from 5 to 0.5 μm (red circles). The best agreement between the model [see (20)] and the measurement results was obtained for $d_{\text{poi}} = \tilde{t}_{\text{diel}} + 11.9$ nm and $q_{\text{co}} = 0.999$. Also shown are results of TCAD simulations of the transfer characteristics (blue circles) and of the surface potential (blue dotted line) for channel lengths from 5 to 0.1 μm; in this case, the best agreement with the model (blue line) was obtained for $d_{\text{poi}} = \tilde{t}_{\text{diel}}$ and $q_{\text{co}} = 0.98$.

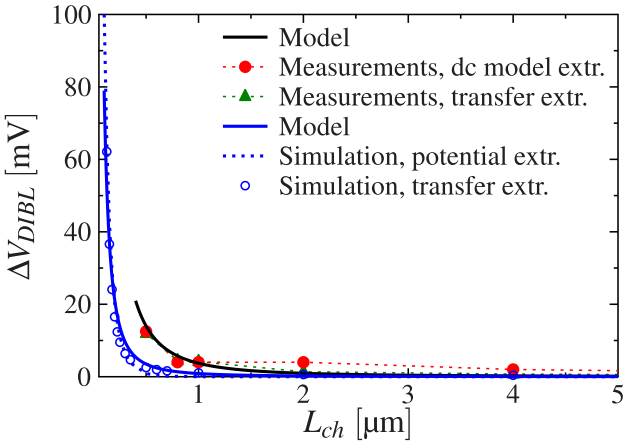

Fig. 8. DIBL-induced threshold-voltage shift ΔV_{DIBL} with decreasing channel length for organic TFTs with channel lengths ranging from 5 to 0.5 μm at a drain–source voltage (V_{ds}) of -1 V calculated using the model presented here (see (21); black line), extracted from the measured transfer characteristics (green triangles) and obtained by fitting the compact dc model presented in [16] individually to the transfer curve of each TFT (red circles). The best agreement between the model [see (21)] and the measurement results was obtained for $d_{\text{poi}} = \tilde{t}_{\text{diel}} + 14.5$ nm and $q_{\text{co}} = 0.999$. Also shown are results of TCAD simulations of the transfer characteristics (blue circles) and of the surface potential (blue dotted line) for channel lengths from 5 to 0.1 μm; in this case, the best agreement with the model (blue line) was obtained for $\tilde{t}_{\text{diel}} + 15$ nm and $q_{\text{co}} = 0.98$.

simulations of the transfer characteristics (blue circles) and of the surface potential (blue dotted line); in this case, the best agreement with the model (blue line) was obtained for an expected $d_{\text{poi}} = \tilde{t}_{\text{diel}}$ and $q_{\text{co}} = 0.98$. In comparison to the extraction of the subthreshold swing and the DIBL, the extraction of the threshold voltage is more challenging, and for the smallest channel length (0.5 μm), we were unable to extract a reliable value of the threshold voltage from the measured TFT characteristics. Nevertheless, the trend of the slight underestimation of the threshold-voltage roll-off by the model can be compensated for by increasing the value of the point of interest d_{poi}.

C. Drain-Induced Barrier Lowering

The DIBL effect describes the influence of the drain–source voltage V_{ds} on the maximum barrier height of the surface potential. Increasing the drain–source voltage leads to a decrease in the surface-potential barrier, causing a shift of the threshold voltage ΔV_{DIBL}. The shift of the maximum-barrier-height position u_{mbh} from the center of the channel toward the source contact is ignored here, and u_{mbh} is derived in the center of the channel, as explained in [14]

$$\begin{aligned}\Delta V_{\text{DIBL}} &= \Phi_{\text{surf}}(V_{\text{ds}}) - \Phi_{\text{surf}}(V_{\text{ds}} = 0\ \text{V}),\\ &= -V_d \frac{d_{\text{poi}}}{\tilde{t}_{\text{diel}}\sqrt{2 + \frac{L_{\text{ch}}^2}{2\tilde{t}_{\text{diel}}^2}}\sqrt{2 + \frac{L_{\text{ch}}^2}{2\tilde{t}_{\text{diel}}^2}(1 - q_{\text{co}})}}.\end{aligned} \tag{21}$$

Fig. 8 illustrates the DIBL-induced threshold-voltage shift ΔV_{DIBL} with decreasing channel length calculated using (21); (black line), extracted from the measured transfer characteristics (green triangles), and obtained by fitting the compact dc model presented in [16] individually to the measured transfer curve of each TFT (red circles). The best agreement between the model and the measurements was obtained for $d_{\text{poi}} = \tilde{t}_{\text{diel}} + 14.5$ nm and $q_{\text{co}} = 0.999$. Also shown in Fig. 8 are results of TCAD simulations of the transfer characteristics (blue circles) and of the surface potential (blue dotted line); in this case, the best agreement with the model (blue line) was obtained for $q_{\text{co}} = 0.98$ and $d_{\text{poi}} = \tilde{t}_{\text{diel}} + 15$ nm, the latter of which is slightly smaller then expected ($d_{\text{poi}} = \tilde{t}_{\text{diel}} + 25$ nm). The same overestimation of the model can be seen when the model is fit to the measurements. The shift ΔV_{DIBL} calculated using the model is determined for $V_{\text{ds}} = -1$ V, and the transfer characteristics were measured for $V_{\text{ds1}} = -0.1$ V and $V_{\text{ds2}} = -3$ V. For all TFTs, regardless of the channel length, the threshold voltage is slightly more negative for $V_{\text{ds1}} = -0.1$ V than for $V_{\text{ds2}} = -3$ V caused by trap-related hysteresis effects [23], as explained in [24]. This DIBL-like shift was extracted from the current–voltage characteristics of the relative long-channel-length TFTs that show channel-length-independent threshold-voltage shifts, where the DIBL effect can be neglected. Finally, for all extraction methods in Fig. 8, the trap-related threshold-voltage shift was subtracted from the total threshold-voltage shift to obtain the true ΔV_{DIBL}.

IV. Verification of Compact DC Model

The model equations derived in Section III for the subthreshold-swing degradation [see (17)], the threshold-voltage roll-off [see (20)] and the DIBL effect [see (21)] can be implemented into any arbitrary compact current model that provides long-channel input parameters for the threshold voltage $V_{T,\text{lc}}$ and the subthreshold swing S_{lc}. For verification, the compact dc model presented in [16] and [25] is used here, and the model equations are implemented as in [14] by substituting the input parameters by (19) and

$$V_{T,\text{total}} = V_{T,\text{lc}} - \Delta V_{T,\text{roll-off}} - \Delta V_{\text{DIBL}}. \tag{22}$$

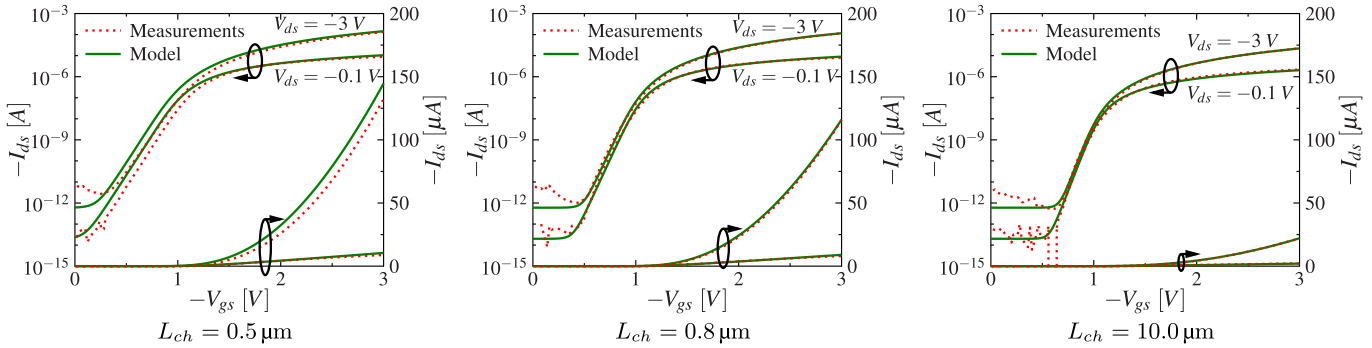

Fig. 9. Results of fitting the enhanced compact current model that includes the short-channel models presented in this work to the measured transfer characteristics of coplanar organic TFTs with channel lengths (L_{ch}) of 0.5, 0.8, and 10 μm. The model parameters are: $q_{co} = 0.999$, $d_{poi,dibl} = 23.45$ nm, $d_{poi,rolloff} = 20.9$ nm and $d_{poi,swing} = 264$ nm.

TABLE I
PARAMETER SETUP OF THE COMPACT DC MODEL

L_{ch}	κ_0	β	μ at $V_{gs} = V_{ds} = -3$ V	$R_c W_{ch}$
$[\mu m]$	$\left[\frac{cm^2 V^\beta}{V s^{-1}}\right]$	[]	$\left[\frac{cm^2}{Vs}\right]$	$[\Omega cm]$
10.0	3	0.4	3.84	38.7
4.0	2.45	0.4	3.14	16.3
2.0	2.2	0.475	2.95	16
1.0	1.8	0.475	2.41	11.5
0.8	1.33	0.49	1.8	11.2
0.5	1.1	0.5	1.5	10.5

In Fig. 9, the compact current model including the short-channel effects derived here is fit to the measured transfer characteristics of coplanar organic TFTs with channel lengths 0.5, 0.8, and 10 μm. The subthreshold swing and the DIBL effect computed using (17) and (21) are in excellent agreement with the measurement results for all channel lengths. Fitting the threshold-voltage roll-off [see (20)] works adequately for channel lengths of 0.8 μm and above, but less so for channel lengths below 0.8 μm. However, even the extraction of the threshold voltage (see Fig. 7) is already quite difficult and somewhat inaccurate at these small channel lengths.

Table I summarizes those parameters of the compact current model which was presented in [16] that are not part of the derived short-channel models in this article, which are not scalable with respect to the channel length and must be fit individually for each transistor. The parameters of the power-law mobility model (μ_0 and β) yield an effective charge-carrier mobility (μ) at $V_{gs} = V_{ds} = -3$ V between 3.8 cm^2/(Vs) for $L_{ch} = 10$ μm and 1.5 cm^2/(Vs) for $L_{ch} = 0.5$ μm, which is similar to the values reported in [20]. In a previously published approach to the empirical modeling of the nonlinear contact effects in organic TFTs, a similar dependence of the channel length on the channel-width-normalized contact resistance $R_c W_{ch}$ in organic TFTs was observed [26], although it was reported there only for TFTs in the staggered device architecture.

The channel-length-independent parameters of the compact current model that was presented in [16] are: The long-channel threshold voltage $V_{T,lc} = -1.02$ V, the trap-related parameter $\alpha_{Traps} = 1.33$, the semiconductor thickness $t_{sc} = 17$ nm, and the fitting parameters that were used in Section III for the short-channel models.

V. CONCLUSION

We have derived analytical and physics-based models for the subthreshold-swing degradation, the DIBL effect, and the threshold-voltage roll-off in coplanar organic TFTs. The models include empirical approaches to compensate the subthreshold swing degradation due to traps. For this, a two-dimensional potential solution of Laplace's equation was derived and applied to extract the potential at the position of the maximum barrier height along the most leaky path of the drain–source current in order to define the short-channel models. Using the models, the subthreshold swing and the DIBL were calculated below the threshold voltage, i.e., in the absence of a gate-field-induced charge-carrier accumulation channel and with the drain current expected to flow along the semiconductor/ambient interface, and hence the maximum barrier height was extracted at this interface. In contrast, the threshold-voltage roll-off was calculated above the threshold voltage, i.e., in the presence of an accumulation channel located in close proximity to the gate-dielectric/semiconductor interface, and thus the maximum barrier height was extracted at this interface. To define the position at which the potential is extracted, the model utilizes the parameter d_{poi}, which defines the distance between the gate electrode and the charge carriers in the center of the channel, measured in the direction perpendicular to the direction of current flow.

The subthreshold swing and DIBL calculated using the model were fit to the measured transfer characteristics of coplanar DNTT TFTs with channel lengths ranging from 0.5 to 10 μm, and good agreement was obtained for all channel lengths. The results of the model were also compared to results of TCAD simulations for channel lengths ranging from 0.1 to 10 μm, also with good agreement. For the threshold-voltage roll-off, good agreement between model and measurement data was obtained only for channel lengths of 0.8 μm or greater. Extracting the threshold voltage for channel lengths below 0.8 μm did not produce useful results. However, when comparing the results of the model to results of TCAD simulations, good agreement was obtained for an expected point of interest d_{poi}. Based on the device-fabrication parameters, the distance between the gate

electrode and the gate-dielectric/semiconductor and semiconductor/ambient interface are 9 and 29 nm, respectively, which are expected to be the values for the point of interest d_{poi} of the threshold-voltage roll-off and DIBL model, respectively. The best agreement with the measurement data was indeed obtained for the DIBL model with a value quite close to that ($d_{\mathrm{poi}} = \tilde{t}_{\mathrm{diel}} + 14.5$ nm), and for the threshold-voltage roll-off model, the value must be slightly increased ($d_{\mathrm{poi}} = \tilde{t}_{\mathrm{diel}} + 11.9$ nm) to achieve an excellent agreement. In contrast, for the subthreshold-swing degradation, the best agreement between model and measurement data was obtained for a d_{poi} value of $\tilde{t}_{\mathrm{diel}} + 255$ nm, which is unrealistically large. One reason is that the verification was performed by comparing the modeling results to the measured transfer characteristics of organic TFTs with different channel lengths and that the trap density at the position of the potential barrier may be different. A parameter extraction of the trap density of each TFT for an expected d_{poi} produced realistic values that increase with decreasing channel length. Another reason may be dynamic charge trapping in the semiconductor that may affect the current–voltage characteristics. Thus, the value for the point of interest d_{poi} for which the best agreement between the subthreshold-swing-degradation model and the measurement data was obtained reflects not only the channel-length dependence of the potential barrier height but also all other physical effects that influence the subthreshold swing and which are affected by the channel length. For the verification of the model using results of TCAD simulations, trapping effects were ignored, and as a result, the subthreshold-swing degradation and threshold-voltage roll-off models are in good agreement with an expected point of interest at $d_{\mathrm{poi}} = \tilde{t}_{\mathrm{diel}} + t_{\mathrm{sc}}$ and $d_{\mathrm{poi}} = \tilde{t}_{\mathrm{diel}}$, respectively. However, the verification of the DIBL model shows that the point of interest must be smaller as expected ($d_{\mathrm{poi}} = \tilde{t}_{\mathrm{diel}} + 15$ nm) in order to compensate a slight overestimation of the model.

Finally, we have been able to demonstrate that the current dc model that was presented in [16] is significantly improved when the newly developed models for the short-channel effects are incorporated; this has been illustrated by fitting results from the new model to the measured current-voltage characteristics of organic TFTs with channel lengths ranging from 0.5 to 10 μm, confirming the scalability of the compact model with respect to the channel length.

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