ENGINEERING

Nanoscale flexible organic thin-film transistors

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Direct-write electron-beam lithography has been used to fabricate low-voltage p-channel and n-channel organic thin-film transistors with channel lengths as small as 200 nm and gate-to-contact overlaps as small as 100 nm on glass and on flexible transparent polymeric substrates. The p-channel transistors have on/off current ratios as large as 4×10^9 and subthreshold swings as small as 70 mV/decade, and the n-channel transistors have on/off ratios up to 10^8 and subthreshold swings as low as 80 mV/decade. These are the largest on/off current ratios reported to date for nanoscale organic transistors. Inverters based on two p-channel transistors with a channel length of 200 nm and gate-to-contact overlaps of 100 nm display characteristic switching-delay time constants between 80 and 40 ns at supply voltages between 1 and 2 V, corresponding to a supply voltage–normalized frequency of about 6 MHz/V. This is the highest voltage-normalized dynamic performance reported to date for organic transistors fabricated by maskless lithography.

INTRODUCTION

Organic thin-film transistors (TFTs) are potentially useful for a variety of flexible electronics applications, including active-matrix displays, sensor arrays, and integrated circuits (*1*–*6*). An important TFT performance parameter is the transit frequency f_T, which can be written as (*7*)

$$f_T = \frac{\mu_0 (|V_{GS} - V_{th}|)}{\left(1 + \frac{\mu_0 (|V_{GS} - V_{th}|) C_{diel} R_C W}{2L}\right) 2\pi L \left(\frac{2}{3} L + 2 L_{ov}\right)} \quad (1)$$

where μ_0 is the intrinsic channel mobility, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, C_{diel} is the unit-area gate-dielectric capacitance, R_C is the contact resistance, W is the channel width, L is the channel length, and L_{ov} are the gate-to-source and gate-to-drain overlaps.

To illustrate the dependence of the transit frequency on the various TFT parameters, solutions to Eq. 1 are plotted in Fig. 1 for critical TFT dimensions (L and L_{ov}) ranging from 0.1 to 10 μm, channel width–normalized contact resistances ($R_C W$) ranging from 10 ohm·cm to 1 kilohm·cm, and intrinsic channel mobilities (μ_0) of 1 and 20 cm^2/Vs. For these calculations, the difference between the gate-source voltage (V_{GS}) and the threshold voltage (V_{th}) was set to a value of 2 V, and the unit-area gate-dielectric capacitance (C_{diel}) was set to a value of 0.7 μF/cm^2, as these are approximately the values for V_{GS}-V_{th} and C_{diel} that are relevant for the experiments presented here. Figure 1 shows that, for contact resistances greater than about 100 ohm·cm, the influence of the intrinsic channel mobility on the transit frequency is relatively weak, while the impact of the contact resistance ($R_C W$) and the critical TFT dimensions (L and L_{ov}) is quite substantial. Improvements of the transit frequency can thus be expected by reducing either the contact resistance (*7*–*9*) or the channel length and the gate-to-contact overlaps (*10*).

How small the channel length and the gate-to-contact overlaps can be made depends to a large extent on the patterning process. The resolution limit of most of the lithography techniques typically used for organic-TFT fabrication, including photolithography (*1*–*4*, *11*–*16*), laser lithography (*17*–*21*), and stencil lithography (*6*–*8*, *22*–*25*), is approximately 1 μm. Organic TFTs fabricated using these techniques have shown transit frequencies up to 160 MHz (at a gate-source voltage of 40 V) on rigid substrates (*17*) and up to 22 MHz (at a gate-source voltage of 12 V) on flexible substrates (*18*), as well as voltage-normalized transit frequencies up to 6.5 MHz/V (45 MHz at a gate-source voltage of 7 V) on rigid substrates (*11*) and 7 MHz/V (21 MHz at a gate-source voltage of 3 V) on flexible substrates (*7*). By combining nanoimprint lithography and self-aligned photolithography, Rothländer *et al.* (*26*), Gold *et al.* (*27*), and Higgins *et al.* (*28*–*30*) fabricated flexible organic TFTs with channel lengths as small as 380 nm, gate-to-contact overlaps as small as 100 nm, and transit frequencies up to 2.8 MHz. For vertical organic permeable-base transistors in which the distance traveled by the charge carriers from the emitter to the collector is defined by a deposited-layer thickness and only the parasitic overlaps are defined by lithography, operation at frequencies up to 100 MHz at a supply voltage of 4 V (25 MHz/V) has been reported (*31*).

Electron-beam lithography is a high-resolution patterning technique that has been used previously to fabricate organic TFTs with channel lengths as small as 10 nm (*32*–*34*), which is within an order of magnitude of the smallest channel length that has been implemented in vertical organic transistors (*35*). However, in these previous reports (*32*–*34*), the TFTs were fabricated on silicon substrates, with the doped silicon serving as a global gate electrode for all TFTs on the substrate, which is not useful for the implementation of integrated circuits. In addition, electron-beam lithography has, to our knowledge, never been used to fabricate organic TFTs on flexible polymeric substrates. Here, we report on the static and dynamic characteristics of low-voltage p-channel and n-channel organic TFTs with channel lengths as small as 200 nm and gate-to-contact overlaps as small as 100 nm fabricated by electron-beam lithography on glass and on flexible polyethylene naphthalate (PEN) substrates. The TFTs have on/off current ratios as large as 4×10^9 and subthreshold swings as small as 70 mV/decade. Unipolar inverters display characteristic switching-delay time constants between 80 and 40 ns at supply voltages between 1 and 2 V.

RESULTS

Device fabrication

The TFTs were fabricated in the bottom-gate, bottom-contact device architecture. The aluminum gate electrodes and the gold source

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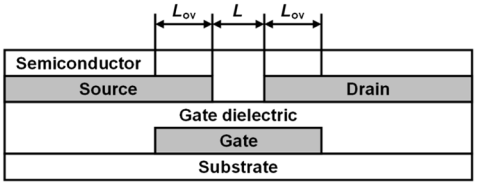
and drain contacts were patterned by electron-beam lithography and liftoff. The gate dielectric is a stack of plasma-grown aluminum oxide (AlO_x) and a phosphonic acid self-assembled monolayer (SAM) with a thickness of 8 nm and a unit-area capacitance of 0.7 μF/cm^2 (*36*). Two different vacuum-deposited small-molecule organic semiconductors, namely, 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT) (*37*) and ActivInk N1100 (*38*), were used for the p-channel and n-channel TFTs, respectively. Before the deposition of the organic semiconductors, the surface of the source and drain contacts was functionalized with a chemisorbed monolayer of either pentafluorobenzenethiol (PFBT) or benzyl mercaptan (BM) to minimize the contact resistance in the p-channel and n-channel TFTs, respectively. A schematic cross section of the TFTs and the molecular structures of the organic semiconductors and the molecules for the contact functionalization are shown in Fig. 2.

Nanoscale flexible p-channel organic TFTs

Figure 3 shows a photograph of a PEN substrate after TFT fabrication, a photograph of an array of 25 organic TFTs on a PEN substrate, a scanning electron microscopy (SEM) image of a TFT, and an SEM image of a part of the channel region of a DPh-DNTT TFT having a channel length of 300 nm and gate-to-contact overlaps of 100 nm. This SEM image also illustrates the characteristic thin-film morphology of the vacuum-deposited DPh-DNTT films (*8*, *39*). The source and drain contacts of all TFTs are designed in a comb layout [eliminating the need for proximity-effect correction during electron-beam lithography (*40*)] with a contact-finger width of 1 μm and a finger-to-finger spacing of 1 μm. The channel width (W) of the TFTs is defined here as the distance between the outermost edges of the two outermost fingers. This is larger than the contact width by roughly a factor of 2. (For example, the TFT shown in the bottom



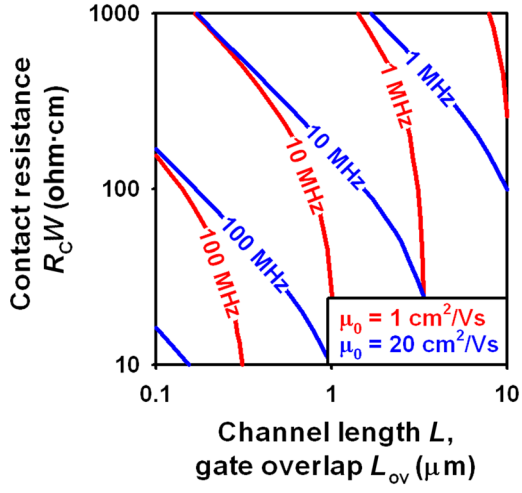


Fig. 1. Transit-frequency dependence on TFT parameters. Contour plot showing the transit frequency (f_T) of a field-effect transistor calculated using Eq. 1 for channel lengths (L) and gate-to-contact overlaps (L_{ov}) ranging from 0.1 to 10 μm, channel width–normalized contact resistances (R_CW) ranging from 10 ohm·cm to 1 kilohm·cm, and intrinsic channel mobilities (μ_0) of 1 and 20 cm^2/Vs. The channel length, the gate-to-source overlap, and the gate-to-drain overlap are assumed to be identical ($L = L_{ov} = L_{ov,GS} = L_{ov,GD}$). The difference between the gate-source voltage (V_{GS}) and the threshold voltage (V_{th}) was set to a value of 2 V, and the unit-area gate-dielectric capacitance (C_{diel}) was set to a value of 0.7 μF/cm^2, as these are approximately the values for V_{GS}-V_{th} and C_{diel} that are relevant for the experiments presented in this work. The graph illustrates that, for contact resistances greater than about 100 ohm·cm, the dependence of the transit frequency on the intrinsic channel mobility is relatively weak, while the impact of the critical device dimensions is quite large.

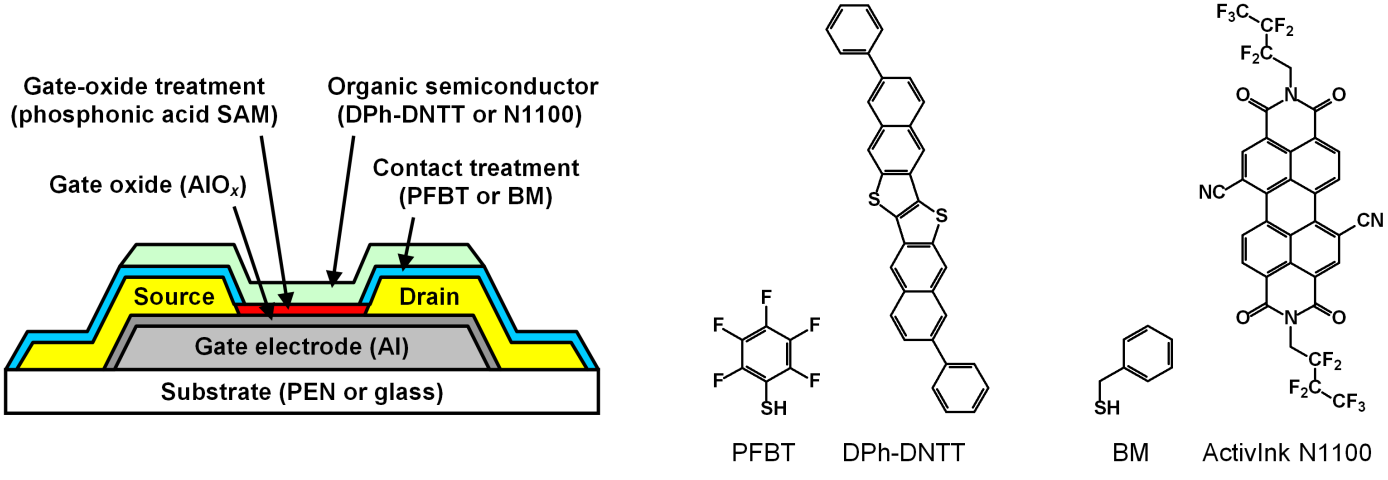


Fig. 2. Device structure. Schematic TFT cross section and structures of the molecules for organic semiconductors and contact functionalization.

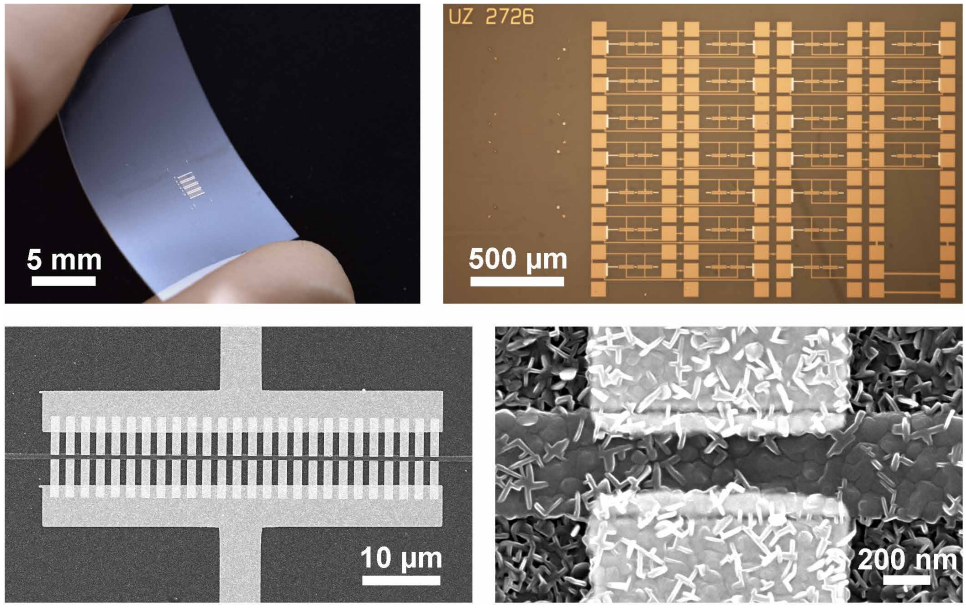


Fig. 3. Flexible nanoscale organic transistors. (**Top row**) Photographs of a flexible PEN substrate with an array of 25 organic TFTs fabricated by electron-beam lithography. (**Bottom row**) Scanning electron microscopy (SEM) images of a TFT having a channel width of 50 µm (left) and of a part of the channel region of a DPh-DNTT TFT having a channel length of 300 nm and gate-to-contact overlaps of 100 nm (right). In the SEM image on the right, the characteristic thin-film morphology of the vacuum-deposited DPh-DNTT films is clearly seen (*8*, *39*).

row of Fig. 3 has a contact width of 26 µm but a channel width of 50 µm.) Because most of the drain current is expected to flow inside the regions bounded by the edges of each pair of contact fingers, as illustrated in figure S6 in (*41*), defining the channel width as the distance between the two outermost fingers would lead to an underestimation of the channel width–normalized transconductance (g_m/W) and an overestimation of the channel width–normalized contact resistance ($R_C W$) by slightly less than a factor of 2. However, as discussed in (*41*), a portion of the drain current flows outside the boundaries defined by the contact edges (i.e., as fringe currents), so depending on how much these fringe currents contribute to the drain current, the underestimation of g_m/W and the overestimation of $R_C W$ will be smaller than a factor of 2.

The measured current-voltage characteristics of p-channel DPh-DNTT TFTs with channel lengths ranging from 200 to 900 nm and gate-to-contact overlaps of 100 or 200 nm fabricated on a flexible PEN substrate are summarized in Fig. 4. The transfer characteristics indicate on/off current ratios between 1×10^8 and 4×10^9, subthreshold swings between 80 and 150 mV/decade, turn-on voltages between 0.0 and 0.4 V, and channel width–normalized transconductances (g_m/W) up to 0.7 S/m (see Table 1). This is the first report of submicrometer channel-length organic TFTs with an on/off current ratio greater than 10^9 and one of the first reports of flexible submicrometer channel-length organic TFTs with a subthreshold swing below 100 mV/decade (*7*, *23*, *42*). The small off-state drain currents, near-zero turn-on voltages, large on/off current ratios, and small subthreshold swings observed here confirm that useful static performance can indeed be obtained in flexible organic TFTs with nanoscale channel lengths, provided that the gate-dielectric thickness is smaller than the channel length by a factor of at least 10 to 20 (*43*, *44*). The critical importance of small off-state drain currents and small subthreshold swings in view of the stringent requirements imposed by mobile or wearable systems regarding low-voltage device operation and ultralow power consumption cannot be overstated.

Contact resistance

To estimate the channel width–normalized contact resistance ($R_C W$), we calculate the channel width–normalized total resistance [$RW = (V_{DS}/I_D)\cdot W$] of the TFT with the smallest channel length (L = 200 nm; W = 80 µm), for which a drain current (I_D) of 1.7 µA was measured at a drain-source voltage (V_{DS}) of −0.1 V and a gate-source voltage (V_{GS}) of −2 V, obtaining a value (RW) of 500 ohm·cm. This value represents the sum of the contact resistance ($R_C W$) and the channel resistance and thus an upper limit of the contact resistance. (For the channel lengths considered here, the channel resistance is insignificant compared to the contact resistance.) The contact resistance of the DPh-DNTT TFTs fabricated by electron-beam lithography reported here is thus smaller than the contact resistance reported in about 80% of all previous publications in which the contact resistance of organic TFTs has been reported (*7*, *45*). It is, however, larger by about an order of magnitude than the contact resistance reported previously for DPh-DNTT TFTs fabricated by stencil lithography (*7*, *8*, *42*). The larger contact resistance of the TFTs fabricated by electron-beam lithography is possibly the result of contamination of the contact surfaces during the liftoff process that follows the electron-beam lithography process, and/or due to the relatively sharp edges of the contacts when these are patterned by electron-beam lithography, rather than stencil lithography (*46*). Figure 1 shows that the larger contact resistance negates most of the benefits of the small channel length and gate overlaps on the expected transit frequency of the TFTs, which implies that future work must focus on reducing the contact resistance, ideally below 10 ohm·cm (*9*).

Low-voltage TFT operation

Figure 5 shows the measured transfer and output characteristics of a p-channel DPh-DNTT TFT with a channel length of 600 nm and gate-to-contact overlaps of 400 nm fabricated on a flexible PEN substrate when measured with maximum gate-source and drain-source

voltages of −1 V. The transfer characteristics indicate a turn-on voltage of 0.0 V, a subthreshold swing of 70 mV/decade, and an on/off current ratio of 3×10^8; this is the largest on/off current ratio reported to date for organic TFTs over a gate-source voltage range from 0 to ±1 V or less (*47*).

Inverters and dynamic performance

To evaluate the dynamic performance of the submicrometer channel-length TFTs, we fabricated unipolar inverters designed in a biased-load circuit topology (*48*). These inverters are based on two p-channel DPh-DNTT TFTs with channel lengths of 200 nm and

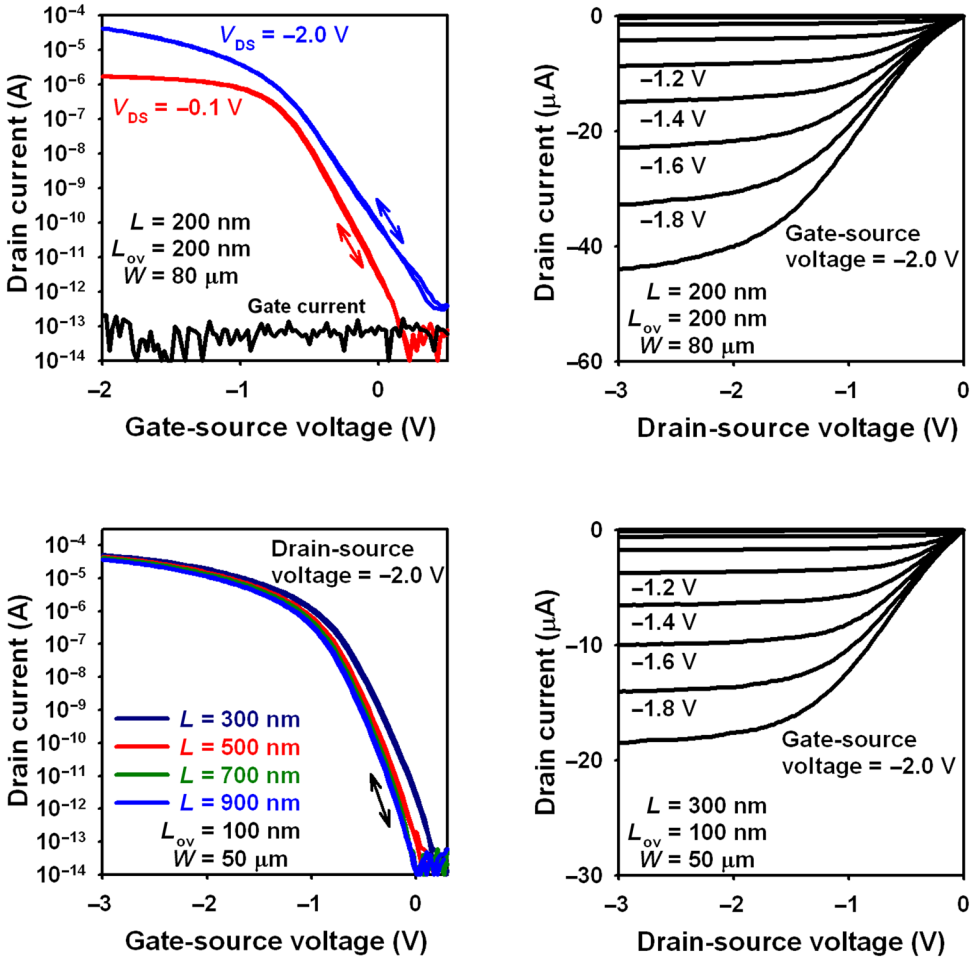


Fig. 4. Current-voltage characteristics of p-channel DPh-DNTT TFTs fabricated on a flexible PEN substrate. (**Top row**) Transfer and output characteristics of a TFT with a channel length of 200 nm, gate-to-contact overlaps of 200 nm, and a channel width of 80 μm. (**Bottom row**) Transfer characteristics of TFTs with channel lengths of 300, 500, 700, and 900 nm, gate-to-contact overlaps of 100 nm, and a channel width of 50 μm and output characteristics of the TFT with a channel length of 300 nm. The on/off current ratios, subthreshold swings, turn-on voltages, channel width–normalized transconductances, and effective charge-carrier mobilities extracted from the transfer characteristics of these TFTs are summarized in Table 1.

Table 1. Static-performance parameters of the p-channel DPh-DNTT TFTs fabricated on a flexible PEN substrate. The table summarizes the performance parameters of the TFTs shown in Fig. 4. [The channel width (*W*) is defined here as the distance between the outermost edges of the two outermost source/drain fingers, which may lead to an underestimation of the channel width–normalized transconductance, depending on the contribution of fringe currents (*41*).]

Channel length *L* (nm)	Gate-to-contact overlap L_{ov} (nm)	On/off current ratio	Subthreshold swing (mV/decade)	Turn-on voltage (V)	Width-normalized transconductance g_m/W (S/m)	Effective charge-carrier mobility μ_{eff} (cm^2/Vs)
200	200	1×10^8	150	0.4	0.7	0.1
300	100	1×10^9	100	0.2	0.6	0.1
500	100	8×10^8	90	0.1	0.5	0.2
700	100	4×10^9	80	0.0	0.5	0.3
900	100	4×10^9	80	0.0	0.4	0.4

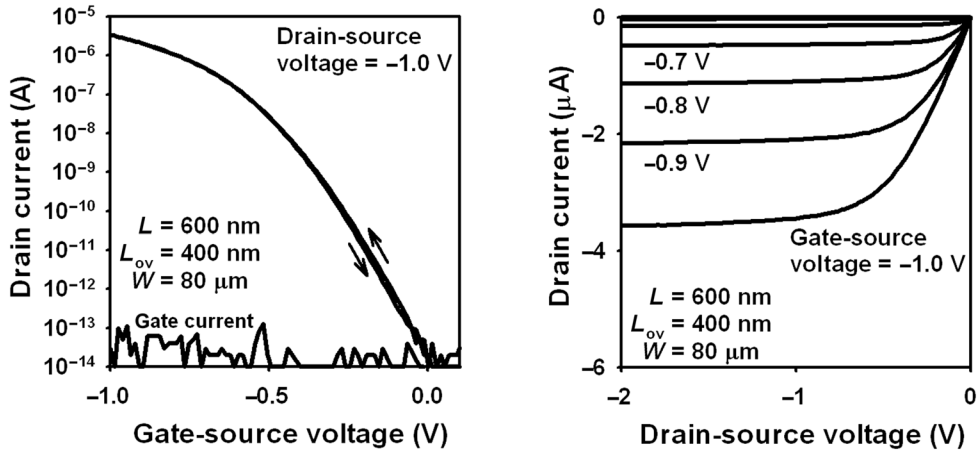


Fig. 5. Low-voltage TFT operation. Current-voltage characteristics of a p-channel DPh-DNTT TFT with a channel length of 600 nm, gate-to-contact overlaps of 400 nm, and a channel width of 80 μm fabricated on a flexible PEN substrate when operated with maximum gate-source and drain-source voltages of −1 V. The transfer characteristics indicate an on/off current ratio of 3×10^8 and a subthreshold swing of 70 mV/decade.

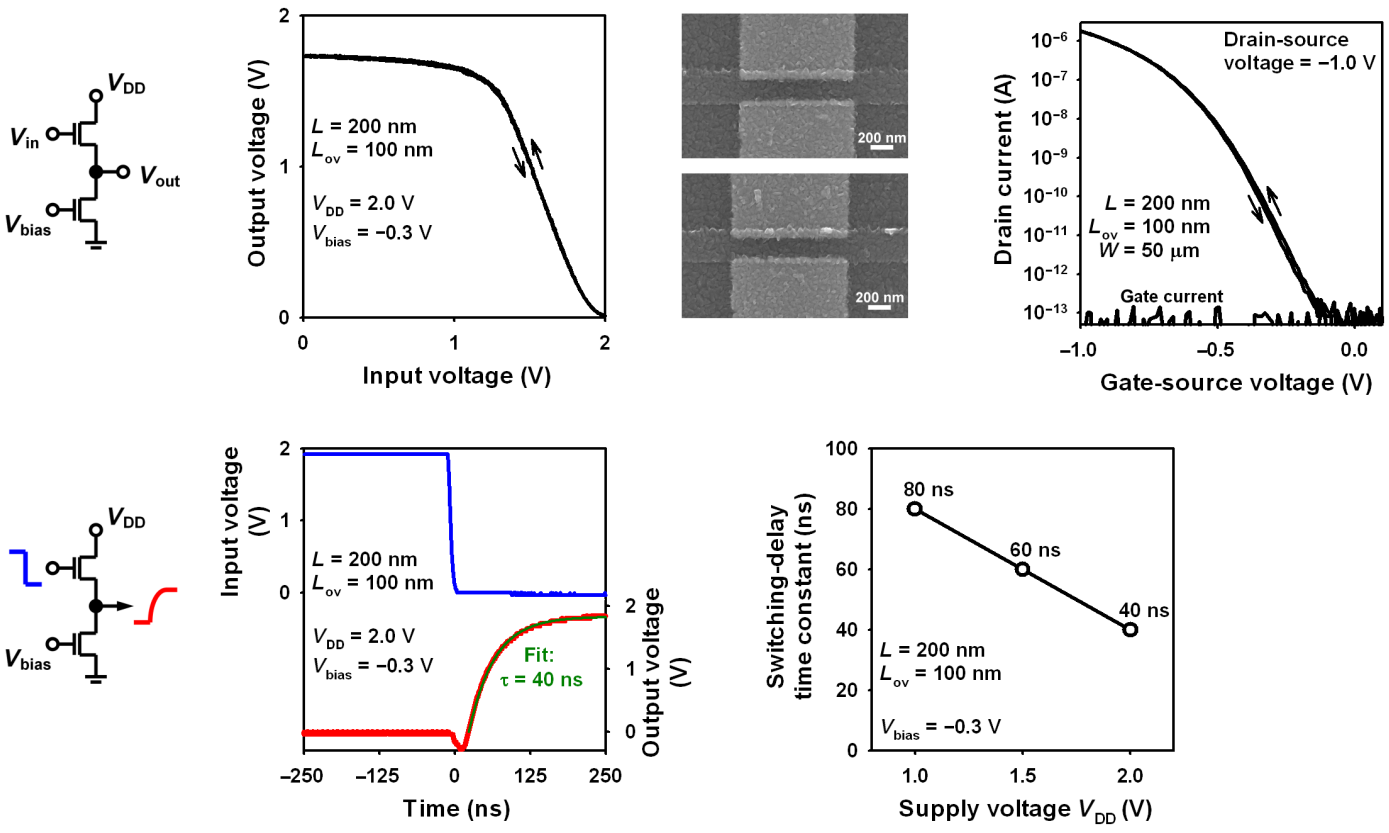


Fig. 6. Inverters and dynamic performance. Static and dynamic characteristics of a biased-load unipolar inverter based on two p-channel DPh-DNTT TFTs with channel lengths of 200 nm and gate-to-contact overlaps of 100 nm fabricated on a glass substrate. (**Top row**) Circuit schematic and static transfer characteristics of the inverter. The drive TFT (connected to V_{DD}) has a channel width of 100 μm (part of the channel region of the drive TFT is shown in the top SEM image), and the load TFT (connected to ground) has a channel width of 20 μm (part of the channel region of the load TFT is shown in the bottom SEM image). The static transfer characteristics indicate a small-signal gain of 2.7. Also shown are the transfer characteristics of an individual TFT with a channel length of 200 nm, gate-to-contact overlaps of 100 nm, and a channel width of 50 μm. (**Bottom row**) To evaluate the dynamic performance of the TFTs, a square-wave voltage (with an amplitude of 1.0, 1.5, or 2.0 V) is applied to the input node of the inverter, and the output response is measured using an oscilloscope. From the output response, characteristic switching-delay time constants of 80, 60, and 40 ns at supply voltages of 1.0, 1.5, and 2.0 V (equal to the input-voltage amplitude) are extracted for the low-to-high transition of the inverter's output voltage.

Table 2. Literature summary of organic TFTs for which operation at frequencies above 10 MHz has been reported. Laser: laser lithography; Vertical: vertical transistor; Photo: photo lithography; Stencil: stencil lithography; e-beam: electron-beam lithography; AlN: aluminum nitride; n/a: not applicable; n/r: not reported. If the gate-to-source and gate-to-drain overlaps are not identical, the average gate-to-contact overlap is given. In references (*11*) and (*7*), on/off current ratios of 10^{10} are shown for TFTs with channel lengths of 6 and 8 μm, respectively.

Reference	Patterning method	Substrate	Operation frequency (MHz)	Operation voltage (V)	Normalized frequency (MHz/V)	Channel length (μm)	Gate overlap (μm)	On/off current ratio	Subthreshold swing (V/decade)
(*17*)	Laser	AlN	160	40	4.0	1.2	0.17	2×10^{2}	10
(*31*)	Vertical	Glass	100	4	25	0.5	n/a	5×10^{4}	0.11
(*11*)	Photo	Glass	45	7	6.4	1.5	1	n/r	n/r
(*57*)	Vertical	Glass	40	8.6	4.7	0.2	n/a	n/r	n/r
(*12*)	Photo	Glass	38	15	2.5	1.5	2	2×10^{9}	0.6
(*13*)	Photo	Glass	27.7	20	1.4	2	2.5	1×10^{6}	2
(*18*)	Laser	Glass	24	15	1.6	1.4	2.7	1×10^{2}	9
(*18*)	Laser	PEN	22	12	1.8	1.2	2.3	5×10^{1}	5
(*7*)	Stencil	PEN	21	3	7.0	0.6	5	1×10^{9}	0.066
(*14*)	Photo	Glass	20	20	1.0	2	1	n/r	n/r
(*22*)	Stencil	Glass	20	20	1.0	2.5	0.5	1×10^{8}	0.8
(*58*)	Vertical	Glass	20	15	1.3	0.8	n/a	1×10^{7}	1
(*19*)	Laser	Glass	20	30	0.7	1.75	3	5×10^{3}	6
(*15*)	Photo	Glass	20	10	2.0	3	2.25	1×10^{9}	0.3
(*16*)	Photo	Glass	19	10	1.9	2	2	1×10^{8}	1
(*20*)	Laser	Glass	19	12	1.6	1.2	2.3	5×10^{4}	2
(*21*)	Laser	PEN	14.4	7	2.1	1	1.7	1×10^{2}	1
(*13*)	Photo	Glass	11.4	20	0.6	2	2.5	1×10^{6}	1
(*23*)	Stencil	PEN	10.4	3	3.5	0.85	5	1×10^{8}	0.07
This work	e-beam	Glass	12.5	2	6.2	0.2	0.1	4×10^{7}	0.07

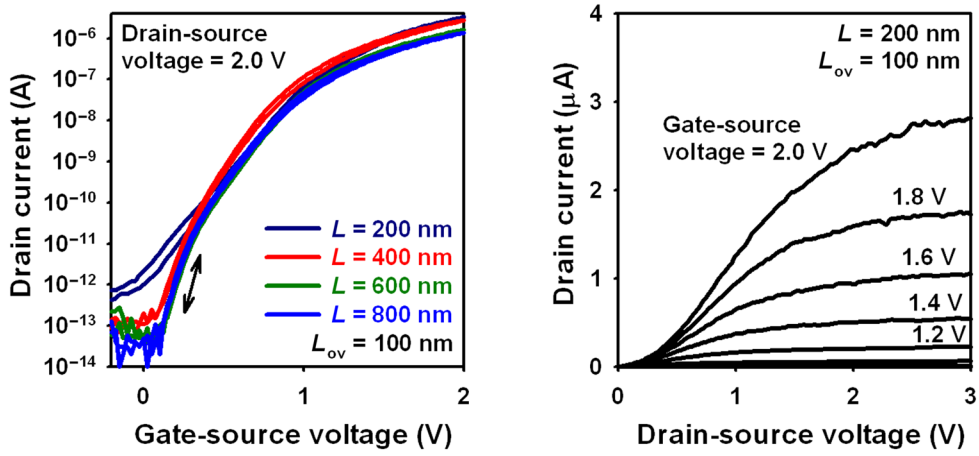


Fig. 7. Transfer and output characteristics of n-channel ActivInk N1100 TFTs fabricated on a glass substrate. The TFTs have channel lengths of 200, 400, 600, and 800 nm and gate-to-contact overlaps of 150 nm. The channel width is 50 μm. The on/off current ratios, subthreshold swings, turn-on voltages, channel width–normalized transconductances and effective charge-carrier mobilities extracted from the transfer characteristics of these TFTs are summarized in Table 3.

Table 3. Static-performance parameters of the n-channel N1100 TFTs fabricated on a glass substrate. The table summarizes the performance parameters of the TFTs shown in Fig. 7. [The channel width (*W*) is defined here as the distance between the outermost edges of the two outermost source/drain fingers, which may lead to an underestimation of the channel width–normalized transconductance, depending on the contribution of fringe currents (*41*).]

Channel length L (nm)	Gate-to-contact overlap L_{ov} (nm)	On/off current ratio	Subthreshold swing (mV/decade)	Turn-on voltage (V)	Width-normalized transconductance g_m/W (S/m)	Effective charge-carrier mobility μ_{eff} (cm^2/Vs)
200	150	5×10^6	200	−0.5	0.2	0.02
400	150	3×10^7	90	−0.3	0.1	0.03
600	150	8×10^7	80	−0.3	0.06	0.03
800	150	1×10^8	80	0.1	0.05	0.04

gate-to-contact overlaps of 100 nm and were fabricated on a glass substrate by electron-beam lithography. Figure 6 shows the circuit schematic and the measured static and dynamic characteristics of such an inverter, as well as the transfer characteristics of an individual TFT with these device dimensions (L = 200 nm, L_{ov} = 100 nm). The TFT characteristics indicate an on/off current ratio of 4×10^7, a subthreshold swing of 70 mV/decade, a turn-on voltage of −0.1 V, a channel width–normalized transconductance of 0.2 S/m, and an effective charge-carrier mobility (μ_{eff}) of 0.1 cm^2/Vs. From the inverter's static transfer curve, a small-signal gain of 2.7 is extracted.

From the inverter's dynamic characteristics, which were measured by applying a square-wave voltage with an amplitude of 1.0, 1.5, or 2.0 V to the input of the inverter while recording the output response using a high-impedance probe and an oscilloscope, characteristic switching-delay time constants (τ) of 80, 60, and 40 ns were extracted for supply voltages of 1.0, 1.5, and 2.0 V (equal to the amplitude of the input voltage), respectively. These switching-delay time constants correspond to equivalent frequencies [$f_{eq} = 1/(2 \cdot \tau)$] of 6.2, 8.3, and 12.5 MHz. A complete literature summary of organic TFTs for which operation at frequencies above 10 MHz has been reported is provided in Table 2.

We would like to compare this experimental result (equivalent frequency of 12.5 MHz at a supply voltage of 2 V) to the transit frequency (f_T) predicted by Eq. 1. Calculating the transit frequency using Eq. 1 requires knowledge of the intrinsic channel mobility of the TFTs (μ_0). A precise value of μ_0 cannot be obtained from the measurement data in Figs. 4 to 6, but we will take as the lower limit the effective charge-carrier mobility of the TFTs with a channel length of 200 nm (0.1 cm^2/Vs) and as the upper limit the intrinsic channel mobility reported previously for DPh-DNTT TFTs fabricated by stencil lithography [5 cm^2/Vs; (*8*)]. For this range of intrinsic channel mobilities (0.1 to 5 cm^2/Vs) and for the contact resistance estimated for the TFTs on this substrate (1 kilohm·cm), Eq. 1 yields transit frequencies of 10.6 MHz for μ_0 = 0.1 cm^2/Vs, 12.9 MHz for μ_0 = 0.5 cm^2/Vs, and 13.5 MHz for μ_0 = 5 cm^2/Vs (V_{GS}-V_{th} = 2 V, C_{diel} = 0.7 μF/cm^2, L = 200 nm, L_{ov} = 100 nm). The experimentally determined equivalent frequency (12.5 MHz) thus falls into the range of transit frequencies predicted by Eq. 1 (10.6 to 13.5 MHz, depending on which value is assumed for the intrinsic channel mobility). Because the equivalent frequency is a large-signal parameter, while the transit frequency is a small-signal parameter, there is no generally applicable relation between these two parameters, but the ratio f_{eq}/f_T has been reported to be about 0.6 across various field-effect transistor technologies (*49*), which is consistent with the results reported here.

Nanoscale n-channel organic TFTs

In addition to p-channel TFTs (based on DPh-DNTT as the semiconductor), we also fabricated n-channel organic TFTs, using Polyera ActivInk N1100 as the semiconductor (*38*, *47*). The measured current-voltage characteristics of n-channel N1100 TFTs with channel lengths ranging from 200 to 800 nm and gate-to-contact overlaps of 150 nm fabricated on a glass substrate are summarized in Fig. 7. The transfer characteristics indicate on/off current ratios up to 10^8, subthreshold swings as small as 80 mV/decade, turn-on voltages between 0.1 and −0.5 V, and channel width–normalized transconductances (g_m/W) up to 0.2 S/m (see Table 3). This is the first time that an on/off current ratio above 10^7 or a subthreshold swing below 100 mV/decade is reported for n-channel organic TFTs with a channel length below 1 μm.

DISCUSSION

The nanoscale TFTs and inverters reported here were fabricated using electron-beam lithography. While the main drawback of electron-beam lithography is its low throughput, this does not preclude the potential of using electron-beam lithography to fabricate organic TFTs and circuits on a larger scale. Just like the throughput of other maskless patterning techniques, such as laser lithography (*17*–*21*) and inkjet printing (*50*), can be greatly enhanced by the implementation of multiple beams or multiple nozzles (*51*), the efficiency of electron-beam lithography can be massively increased as well by implementing arrays of individually addressable electron beams (*52*, *53*). These considerations notwithstanding the primary purpose of the work reported here was not to suggest electron-beam lithography as a method for the mass production of organic TFTs, but rather to confirm that organic TFTs with channel lengths and gate-to-contact overlaps in the range of a few hundred nanometers fabricated on flexible plastic substrates can provide useful static performance, including near-zero turn-on voltages as well as off-state drain currents, on/off current ratios, and subthreshold swings comparable to the best values reported for long-channel organic TFTs.

In summary, we have used direct-write electron-beam lithography to fabricate p-channel and n-channel organic TFTs with channel lengths as small as 200 nm and gate-to-contact overlaps as small as 100 nm on glass and on flexible polymeric substrates. The TFTs have on/off current ratios as large as 4×10^9 and subthreshold swings as small as 70 mV/decade. Unipolar inverters display a characteristic switching-delay time constant of 40 ns at a supply voltage of 2 V, corresponding to a supply voltage–normalized frequency of about 6 MHz/V. Better dynamic performance can be expected by reductions

of the contact resistance; for example, for a contact resistance of 10 ohm·cm [the smallest contact resistance reported for organic TFTs (*7*)], a transit frequency above 100 MHz at 2 V can be expected.

MATERIALS AND METHODS

Substrates and device architecture

The TFTs were fabricated in the bottom-gate, bottom-contact (inverted coplanar) device architecture on glass or 125-μm-thick flexible PEN substrates (Teonex Q65 PEN).

Gate electrodes and gate dielectric

To define the gate electrodes, the substrate was coated with a two-layer resist consisting of a bottom layer of poly(methyl methacrylate) (PMMA) having a molecular weight of 200 kg/mol and a thickness of 200 nm (Allresist AR-P 641.05) and a top layer of PMMA having a molecular weight of 950 kg/mol and a thickness of 120 nm (Allresist AR-P 671.025). The purpose of using a two-layer resist is to create a reentrant (undercut) profile to enable clean liftoff of the excess metal. Electron-beam lithography was performed using a Raith eLINE (electron beam voltage, 20 kV; exposure dose, 370 μC/cm^2) or a JEOL JBX6300FS (electron beam voltage, 100 kV; exposure dose, 850 μC/cm^2). The resist patterns were developed in a 2-propanol solution of methyl isobutyl ketone (MIBK). Aluminum with a thickness of 30 nm was deposited by thermal evaporation in vacuum (background pressure, 10^{-7} mbar; deposition rate, 2 nm/s); this layer has a surface roughness of about 1 nm (*54*). The aluminum surface was exposed to oxygen plasma (oxygen flow rate, 30 standard cubic centimeters per minute; oxygen partial pressure, 10 mTorr; plasma power, 200 W; plasma duration, 60 s) to produce an aluminum oxide (AlO_x) gate dielectric with a thickness of about 6 nm (*36*). Patterning of the gate electrodes was completed by lifting off the excess metal in *N*-ethyl-2-pyrrolidone (NEP; Allresist Remover AR 300-70).

Source and drain contacts

To define the source and drain contacts, the substrate was again coated with a two-layer PMMA resist, followed by electron-beam lithography and development in MIBK. Titanium with a thickness of 0.3 nm (to improve adhesion) and gold with a thickness of 30 nm were sequentially deposited by thermal evaporation in vacuum (background pressure, 10^{-7} mbar; deposition rate, 0.03 nm/s). Patterning of the source and drain contacts was completed by liftoff in NEP.

Monolayer functionalization of the gate dielectric and the source/drain contacts

To promote a favorable thin-film morphology of the small-molecule organic semiconductors in the channel region and on the surface of the source/drain contacts (*8*), the substrate was first immersed into a 2-propanol solution of an aliphatic phosphonic acid, allowing the formation of a hydrophobic SAM on the surface of the AlO_x gate dielectric. For the p-channel TFTs, we used *n*-tetradecylphosphonic acid (PCI Synthesis, Newburyport, MA, USA) (*36*), and for the n-channel TFTs, a mixture of 25% *n*-octadecylphosphonic acid (PCI Synthesis, Newburyport, MA, USA) and 75% 12,12,13,13,14,14,15,15,16,16,17,17,18,18,18-pentadecafluoro-octadecylphosphonic acid (synthesized by Matthias Schlörholz, Heidelberg, Germany) (*47*). The phosphonic acid SAM has a thickness of approximately 2 nm, and the hybrid AlO_x/SAM gate dielectric separating the organic semiconductor from the gate electrodes has a total thickness of about 8 nm and a unit-area capacitance of 0.7 μF/cm^2 (*36*, *47*). The substrate was then immersed into an ethanol solution of a thiol or mercaptan to functionalize the surface of the Au source and drain contacts with a chemisorbed monolayer that helps to minimize the contact resistance of the TFTs (*7*, *8*). PFBT and BM (both from TCI) were used for the p-channel and n-channel TFTs, respectively. The monolayer treatments can be performed in reverse order [by immersing the substrate first into the thiol solution to functionalize the contacts and then into the phosphonic-acid solution to functionalize the gate oxide (*55*)]; how this might affect the TFT characteristics was not investigated here.

Organic semiconductors

In the last process step, the organic semiconductor was deposited by thermal sublimation in vacuum (background pressure, 10^{-7} mbar; deposition rate, 0.03 nm/s) through a manually aligned stencil mask (*24*). The small-molecule semiconductors DPh-DNTT (Nippon Kayaku; provided by K. Ikeda, Y. Sadamitsu, and S. Inoue) and *N*,*N*′-bis(2,2,3,3,4,4,4-heptafluorobutyl)-1,7-dicyano-perylene-(3,4:9,10)-tetracarboxylic diimide [PTCDI-$(CN)_2$-$(CH_2C_3F_7)_2$; ActivInk N1100; Polyera Corp., Skokie, IL, USA] were used for the p-channel and n-channel TFTs, respectively (*37*, *38*). During the organic-semiconductor deposition, the substrate holder was heated to a temperature of 90°C (DPh-DNTT) or 140°C (N1100). Given the poor thermal stability of thiols on gold (*56*), it is likely that the BM would desorb from the surface of the source/drain contacts if subjected to a temperature of 140°C. However, because of the substrates' low thermal conductivity, the temperature of the substrate's front surface is likely to be lower than the temperature of the substrate holder. Using contact-angle measurements, we have confirmed that the BM monolayers are still present on the gold surfaces after the substrate holder had been heated to a temperature of 140°C for a duration of 1 hour in vacuum. The actual temperature on the front surface of the substrates during the organic-semiconductor deposition is not known, but it is possibly no higher than approximately 100°C.

Characterization

All electrical measurements were performed in ambient air at room temperature using a manual probe station. The static output and transfer characteristics of the TFTs and inverters were recorded using an Agilent 4156C Semiconductor Parameter Analyzer. The dynamic characteristics of the inverters were recorded using a Keysight 33622A Waveform Generator, a Textronix TDS 1001B Digital Oscilloscope, and a GGB Industries Model 19C Picoprobe.

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