

play a determining role in whether the

device will work successfully as an SGT,

or just as a low-current, poor-performance TFT. The absence of this essential element

is likely to lead to: unimpressive electrical

characteristics that do not get reported;

consternation among researchers; and the

premature shutting-down of promising

SGT operation when deciding on the fab-

rication process. Using examples from

the growing literature^[19] and recently fabricated devices, we describe the tell-tale characteristics of unoptimized contact-

In this study, we show how the saturation coefficient γ can be tuned to enhance

The Secret Ingredient for Exceptional Contact-Controlled Transistors

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Contact-controlled transistors are rapidly gaining popularity. However, simply using a rectifying source contact often leads to unsatisfactory operation, merely as a thin-film transistor with low drain current and reduced effective mobility. This may cause otherwise promising experiments to be abandoned. Here, data from literature is analyzed in conjunction with devices that have been recently fabricated in polysilicon, organic and oxide semiconductors, highlighting the main factor in achieving good saturation, namely keeping saturation coefficient γ well below 0.3. Secondary causes of suboptimal electrical characteristics are also discussed. Correct design of these alternative device structures will expedite their adoption for high gain, low-frequency applications in emerging sensor circuits.

1. Introduction

The reduction of contact effects in thin-film transistors (TFTs) is a principal concern for achieving high operating frequencies, especially in scaled devices with emerging materials.^[1–7] However, in many focused applications, high transit frequency is not critical.^[8–11] Making the engineering decision to rely on the source contact area as the main control mechanism of current control may bring operational benefits that more than outweigh the drawbacks.^[9,12–15] Devices such as the source-gated transistor (SGT) are rapidly gaining interest.^[9,16–19] as they trade off switching frequency for improved gain, saturation characteristics and stability.^[20–22]

While the general recipe for making such devices is straightforward, a crucial element is frequently overlooked. Specifically, the electrostatic properties of the layers making up the device

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202101101.

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DOI: 10.1002/aelm.202101101

controlled behavior and their relationship to choices regarding materials or processes. Making these critical design requirements explicit will expedite SGT optimization and their rapid adoption for high-gain, low-frequency applications.

avenues of work.

2. Source-Gated Transistor Principles

Source-gated transistors (SGTs)^[13,16,23] are thin-film devices using a staggered electrode configuration in which the gate electrode overlaps the source (**Figure 1a**). The source contact to the semiconductor is designed to produce a moderate energy barrier, which serves as the current-control mechanism. As staggered-electrode configurations are finding their way into production, the SGT architecture is rapidly gaining in popularity.^[19] Indeed, a burst of recent activity has led to publications featuring devices in IGZO,^[24] DNTT,^[25] MoS₂,^[26] and In₂O₃.^[27]

At first sight, the energy barrier induced at the source is responsible for directly controlling the drain current in the device. Under the vertical electric field created by the gate, barrier modulation occurs and current increases,^[31] yet in practice the process is confounded by the existence of the lateral electric field from the drain.^[9,32] Indeed, the principal role of the source barrier is to enable the semiconductor layer to be fully depleted by a moderate drain-source voltage at the edge of the source closest to the drain.^[13]

3. SGT Saturation in Practice

The defining features of SGT output characteristics are low saturation voltage,^[9] flat saturation region^[16,20] and independence of channel length^[16,33,34] (Figure 1). The depleted semiconductor www.advancedsciencenews.com





Figure 1. Source-gated transistor (SGT) structure and output characteristics. a) Schematic cross-section of a staggered top-gate SGT, emphasizing the capacitive divider at the edge of the source in the inset. Output characteristics from published literature, in various material systems, reproduced with permission: b) low temperature polysilicon (LTPS) SGT (reprinted from Ref. [9] under the Creative Commons CC-BY-NC-SA license); c) InGaZno (IGZO) with graphene contact SGT (reprinted from Ref. [28] with the permission of AIP publishing); d) silicon nanowire (Si NW) SGT (reprinted from Ref. [29] under the Creative Commons CC BY license); e) ZnO nanosheet (NS) SGT (reprinted from Ref. [30] under the Creative Commons CC BY license); f) IGZO SGT with Schottky contact (reprinted from Ref. [16] under the Creative Commons CC BY license).

at the edge of the source forms a capacitive voltage divider with the gate insulator.^[14,22,34] This pins the voltage under the source edge at a value

$$V_{SAT1} = K + (V_{GS} - V_{th}) \cdot \gamma \tag{1}$$

where *K* is a constant which depends on the state of free charge in the semiconductor and

$$\gamma = \frac{C_{\rm i}}{C_{\rm i} + C_{\rm s}} < 1 \tag{2}$$

is the saturation coefficient, with $C_i = \varepsilon_i/t_i$ and $C_s = \varepsilon_s/t_s$ as the insulator and semiconductor capacitances per unit area, respectively.^[16,23,34]

When $V_{SAT2} = V_{GS} - V_{th}$, the channel pinches off at the drain end in the usual manner, where V_{GS} and V_{th} are the gate-source voltage and threshold voltage, respectively (see Figure 1c).

Contrary to conventional TFT design rules, a relatively low gate-insulator capacitance (i.e., low permittivity ε_i or large insulator thickness t_i) is preferred to attain $\gamma \ll 1$, so that draincurrent saturation can occur at very low drain-source voltages.

Rearranging Equation 2 yields

$$\frac{t_{\rm i}}{t_{\rm s}} = \frac{1 - \gamma}{\gamma} \frac{\varepsilon_{\rm i}}{\varepsilon_{\rm s}} \tag{3}$$

which allows us to plot the γ values extracted from the fabrication methods used in literature (**Figure 2**a). The devices shown in Figure 1 all have exemplary characteristics and low saturation coefficients ($\gamma < 0.2$). Indeed, the measured $\partial V_{\text{SAT1}}/\partial V_{\text{GS}}$







Figure 2. Saturation coefficient γ plays an essential role in the electrical characteristics of SGTs. a) Calculated γ as a function of semiconductor and gate insulator permittivities for devices in a variety of material systems found in literature, as well as fabricated organic (DNTT) and LTPS transistors with P or BF₂ barrier modification implants. The plot identifies permittivity ratios ($\varepsilon_i/\varepsilon_s$) of frequently used semiconductor/insulator combinations and facilitates choosing the minimum insulator thickness (t_i) required to achieve a certain γ value, given a material system and semiconductor layer thickness (t_s). b) Deviations from the calculated γ values have been observed, and these discrepancies are usually larger in devices with larger γ . c) Saturation may occur at higher voltages than predicted by the value of γ if the charge density in the semiconductor is too high, or the contact barrier is too low to allow full depletion of the semiconductor at the edge of the source closest to the drain.

for these devices reliably matches the calculated γ value for each case (Figure 2b).

In practice, the calculated γ does not always result in commensurate variations of V_{SAT1} with V_{GS} . Poorly chosen device electrostatics, fixed and free charges, layer nonuniformity, barrier nonuniformity, and low barrier (preferred for high current) lead to higher $\partial V_{\text{SAT1}}/\partial V_{\text{GS}}$ than expected. This is shown schematically in Figure 2c.

4. Challenges for High-Quality Saturation

Devices deliberately designed with a source barrier frequently produce characteristics substantially inferior to those in Figure 1. Most often, this is a result of a poorly chosen γ (Figure 2).

We have fabricated organic transistors with Ohmic contacts based on the small-molecule semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b] thiophene (DNTT),^[35] which routinely shows carrier mobility above 3 cm² V⁻¹ s⁻¹ and channel-width-normalized contact resistance below 500 Ω cm when Au is used for the source and drain contacts (**Figure 3**a).

By choosing a contact metal other than Au, we induced a barrier at the source. Yet aside from the appearance of a nonlinear region near the origin, the output characteristics of these Cr/Au-contact TFTs saturated in a FET-like manner, with a measured $\partial V_{\text{SATI}}/\partial V_{\text{GS}} \approx 1$. Calculating the saturation coefficient for these devices yields $\gamma = 0.84$, a comparatively large value but expectedly so, given the high dielectric capacitance (700 nF cm⁻²) produced by the thin gate insulator (t_i about 8 nm). As a consequence, the device has FET-like saturation. Simply creating a rectifying contact is not sufficient to achieve SGT characteristics and operation.

We therefore fabricated additional DNTT TFTs with a thicker, lower-permittivity gate insulator (Figure 3b), having a gate-dielectric capacitance of approximately 34 nF cm⁻² and thus a smaller predicted $\gamma \approx 0.21$. Transistors with Cr/Au contacts showed the largest drain current and mobility (2 cm² V⁻¹ s⁻¹, comparable with 2.1-3.0 cm² V⁻¹ s⁻¹ obtained from the previous devices with high specific gate capacitance), and a $\partial V_{SAT1}/\partial V_{GS} \approx 1$. The high mobility and typical TFT saturation behavior indicate that these devices are effectively operating in Ohmic mode, and not as SGTs, contrary to expectations. The Cr work function, 4.5 eV, should create a sizeable energy barrier, which would pinch off the source. The explanation is likely a shift in the shadow mask position between the Cr and Au evaporations, leading to the presence of Au at the edge of the source electrode closest to the drain, instead of Cr. This eventually would result in the absence of the desired large energy barrier, and with it, the inability of the contact to pinch off the semiconductor and achieve low-voltage saturation. This Au contact area would also be responsible for high charge injection density at the source. The high extracted values for effective mobility corroborate this hypothesis.

Transistors with Cu/Au, Ti/Au, and Al/Au contacts showed relatively lower drain current and reduced mobility of 1.3, 0.27





Figure 3. Color plots represent original data, while grayscale graphs are reproduced from literature, with permission. a) Organic DNTT transistors with a gate-dielectric capacitance of \approx 700 nF cm⁻² have a large saturation coefficient, $\gamma = 0.84$, which leads to FET-like saturation whether either Ohmic (Au) or rectifying (Cr/Au) contacts are used. b) Organic DNTT devices with a gate-dielectric capacitance of \approx 34 nF cm⁻² and Cr/Au, Cu/Au, Ti/Au, Al/Au show a reduction in drain current with decreasing source-metal work function. Transistors with Cr/Au sources exhibit FET-like behavior, while the expected SGT-like saturation is seen in the low work function realizations. c) LTPS SGTs, comprising a P barrier lowering implant at the source, demonstrate higher than expected saturation voltage, due to the inability of the source barrier to fully deplete the semiconductor at the edge of the source (reprinted from Ref. [16] under the Creative Commons CC BY license). e) ZnO SGT in which high excess charge leads to high output conductance in saturation and inability to turn off completely. f) MoS₂ SGT with poor output conductance between V_{SAT1} and V_{SAT2}, due to suboptimal lateral field screening (reprinted from Ref. [36] with permission from Elsevier). g) IGZO SGT with inkjet-printed contacts, demonstrating the same behavior as (f) (reprinted from Ref. [37] under the Creative Commons CC BY license).

and 0.015 cm² V⁻¹ s⁻¹, respectively. This trend is consistent with the reducing metal work function (4.5–5.5, 4.33, and 4.1–4.3 eV, respectively). Although the metal work function is not a precise indicator of contact barrier height, lower work functions result in lower current density. Additionally, in all cases, the measured $\partial V_{\text{SAT1}}/\partial V_{\text{GS}} \approx 0.5$ indicates substantially earlier saturation than would be expected of a conventional TFT. These observations are fully consistent with SGT operation. The disagreement with

the calculated γ is not unique to these devices. As we will show next, correctly choosing the design parameters to obtain a low γ is the first of a series of strategies that contribute to drastically improving SGT output characteristics.

First, the source pinch-off will occur once the semiconductor is fully depleted, and, at lower drain-source voltages, the drain current cannot exceed the envelope defined by the current capability of the semiconductor channel in series with the barrier



(Figure 2c). For a long channel, the source is initially more conductive than the source-drain gap and will only reach the saturation current at a drain-source voltage higher than the expected V_{SAT1} . This explains the discrepancy between the measured and calculated values in the DNTT devices in Figure 3b with a comparatively large 100 μ m channel length.

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Second, and for similar reasons, the source-barrier height needs to be sufficiently high. As shown in Figure 3c, a transistor otherwise identical to the LTPS SGT^[9] in Figure 1b but with a substantially lower source barrier, produced $\partial V_{SAT1}/\partial V_{GS} \approx 0.3$, much higher than the calculated γ of 0.04. Here, the lower barrier is more conductive and current saturates at a higher reverse bias, once again in a similar manner to the qualitative description of Figure 2c. A similar reasoning may be followed to account for the discrepancy observed in Figure 2b for the IGZO SGTs with MoCr contacts.^[24]

These constraints, brought about by the interplay between the relative conductivities of the source region and FET channel, are generally responsible for a deviation from the calculated γ . We visually illustrate this in Figure 2b. It is also apparent that devices with lower γ values usually suffer less deviation from expected behavior; in the output characteristics, the maximum allowable current envelope of the FET channel is steeper at low drain-source voltages. Data from numerous material systems leads to the following rule of thumb: successful designs should aim for γ values significantly below 0.3, and preferably under 0.1.

Due to a related effect, poorly saturating curves are also frequently found when the semiconductor is comparatively thick, even if the relative semiconductor and insulator capacitances are well chosen. This is attributable to the inability of the semiconductor layer to reach full depletion under the given biasing condition, and manifests itself as a large output conductance (sloping saturated curves) in the region above $V_{\text{SATI}}^{[16]}$ (see Figure 3d). A full treatment is found in Ref. [16] (Supporting Information).

Achieving full source pinch-off may also be inhibited if the semiconductor layer has substantial excess charge, or if the insulator interface creates a surface doping effect. When this occurs, the transistor also tends not to switch off well, due to the enduring presence of a conduction path between source and drain. A set of solution-processed ZnO SGTs we have recently fabricated presented this behavior (Figure 3e). Here, the saturation voltage change with $V_{\rm GS}$ appears to be in the order of 0.25 V/V and the drain current reaches a relatively modest 20 nA μ m⁻¹, indicating the dominance of contact effects. Nevertheless, the saturation performance is poor, with a linear increase of drain current with drain voltage, explained by the inability of the reverse-biased source barrier to fully deplete the semiconductor layer.

Finally, poor saturation can also occur due to ineffective screening of the source from the lateral field induced by the drain (Figure 3f,g).^[32] This effect is generally seen in short-channel devices, in which the lateral (drain) electric field competes in magnitude with the gate field normal to the source. In such cases, V_{SAT1} is clearly defined in the output characteristics, but the transistor has poor gain above V_{SAT1} , as full saturation only occurs above V_{SAT2} . For all practical purposes, the device operates as a conventional TFT with reduced current

and mobility. General mitigation strategies include increasing the source injection area^[34] and providing lateral field relief via electrode patterning^[32] or local doping.^[20,38] Specifically, in contrast to the devices in Guo et al.,^[36] Liu et al.^[26] obtain record intrinsic gain figures by: improving the gate control via a higher dielectric capacitance; using Pt to create a relatively high barrier at the source contact; operating the device at low gate overdrive voltage where the barrier pull-down is minimized; and incorporating an essential field relief structure.^[32]

5. Outlook for Successful SGT Realization

As evidenced by measurements of devices we have recently fabricated, simply designing TFTs with rectifying source contacts does not inevitably lead to favorable source-gated transistor operation. This is confirmed by examples from literature, and it is very likely that, faced with suboptimal characteristics, many authors may choose to forgo publication, and may altogether halt this line of research. Our intention here is to show that awareness of the various limiting factors makes possible the realization of high-performance contact-controlled devices with ease.

To summarize, in aiming for superior SGT characteristics, it is of critical importance to choose materials which: are compatible within the process and application; have suitable permittivities; and are deposited with layer thicknesses calculated to yield γ of at most 0.3, preferably smaller than 0.1. A simple recipe for design in a given material system would involve first deciding on the minimum semiconductor thickness acceptable for the process and on the desired γ . The minimum insulator thickness is then obtained by rearranging Equation 3

$$t_{\rm i} = \frac{1 - \gamma}{\gamma} \frac{\varepsilon_{\rm i}}{\varepsilon_{\rm s}} t_{\rm s} \tag{4}$$

For example, to reach $\gamma < 0.1$, organic transistors such as the ones presented in Figure 3 with a 20-nm-thick semiconductor layer, would require the gate insulator to be thicker than 463 nm when utilizing Al₂O₃, but only 201 nm if SiO₂ was used instead. An IGZO/Al₂O₃ transistor with identical 20 nm active layer would only require 101 nm insulator thickness.

From Figure 2a, it is clear that the most convenient way of designing SGTs is by using high permittivity, thin semiconductor layers. As such, the relatively high $\varepsilon_s = 16$ of IGZO makes it an ideal candidate for facile realization of SGT-type devices. Conversely, the nanometer-sale active layers achievable in some organic semiconductors or MoS₂ allow them to produce excellent devices despite the relatively low material permittivity.

The ideal SGT combines low permittivity insulators with high permittivity semiconductors. IGZO, Silicon, Germanium, InN or InAs active layers and air/vacuum gaps represent the ultimate match.

In the dialog between designers and process engineers, it may be convenient to discuss designs in terms of layer capacitances. If so, the conditions can be expressed equivalently as

$$\frac{C_{\rm s}}{C_{\rm i}} = \frac{1 - \gamma}{\gamma} \tag{5}$$



In conceiving contact-controlled devices, one should be mindful of the trade-off between low γ values and gate-source voltages required, given the reduced insulator capacitance as γ increases. Even with the correct sizing and material, care should also be taken, to: ensure optimal interplay between barrier height and channel length; reduce bulk and interface charge, which may prevent source pinch-off; and minimize the detrimental consequences of lateral electric fields.

Contact-controlled device research is witnessing an unmistakable upsurge. By following these simple but critical design rules, their valuable properties can be utilized to their potential. High-gain, low-frequency analog applications can be designed for a vast range of emerging applications: innovative displays, printed sensor front-ends, disposable low-power wearables, and flexible IoT devices.

6. Experimental Section

Organic Transistor Fabrication: Organic transistors were fabricated in the inverted staggered (bottom-gate, top-contact) device architecture using the small-molecule semiconductor DNTT (Sigma Aldrich).^[35] The organic transistors were fabricated either on silicon substrates or on flexible polyethylene naphthalate (PEN) with a thickness of 125 µm (Teonex Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, U.K.). For the organic transistors fabricated on silicon substrates, the heavily doped silicon serves as both the substrate and a common gate electrode. In these TFTs, the gate dielectric is a stack of 100-nm-thick silicon dioxide grown by thermal oxidation, 8-nm-thick aluminum oxide deposited by atomic-layer deposition (ALD) and a self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid (PCI Synthesis, Newburyport, MA, USA)^[39] with a unit-area capacitance of 34 nF cm⁻². For the organic transistors fabricated on flexible PEN, patterned gate electrodes are prepared by depositing 30-nm-thick aluminum through a shadow mask (CADiLAC Laser, Hilpoltstein, Germany).^[40] The gate dielectric is a stack of 7-nm-thick aluminum oxide grown by plasma oxidation and an *n*-tetradecylphosphonic acid SAM with a unit-area capacitance of 700 nF cm⁻². For all organic transistors, nominally 25-nm-thick DNTT was deposited by thermal sublimation in vacuum with a deposition rate of 0.3 Å $\rm s^{-1}$ and with the substrate held at a temperature of 60 °C. For the source/drain contacts, either Au with a thickness of 30 nm or a stack of either Cr, Cu, Ti, or Al (with a thickness of 30 nm) followed by Au (also having a thickness of 30 nm) was deposited by thermal evaporation in vacuum with a rate of 0.3 Å s^{-1} . The organic transistors have a channel length of 100, 150, or 200 μ m and a channel width of 200 μ m.

ZnO Solution Preparation: ZnO solgel solution with a final concentration of 0.1 M in 2-methoxyethanol (99.8%, anhydrous, Sigma Aldrich UK) was prepared using zinc acetate dihydrate (\geq 98%, Sigma Aldrich UK) as the ZnO precursor and ethanolamine (\geq 99%, Sigma Aldrich UK) as the stabilizer (molar ratio precursor: stabilizer 1:1). The solution was immediately transferred to a hot plate at 60 °C and stirred continuously for 2 h in air ambient, followed by a minimum of 4 d at room temperature (RT) to complete a stable sol formation. The solution was used for spin coating in its sol form (clear solution) before white particulates appeared.

ZnO Transistor Fabrication: The ZnO solution was used as the semiconductor in solution processed top contact bottom gate transistor devices with a Si/SiO₂/ZnO/MoO₃/Cr/Au structure. To fabricate the devices, first, p-doped Si wafers with 300 nm layer of thermally grown SiO₂ insulator were cleaned acetone, IPA and DI water subsequently (15 min each) in an ultrasonic bath, followed by O₂ plasma treatment (100 W, 5 min). Next, the ZnO solgel solution was spin coated on the Si/SiO₂ substrates in a 2-step process at 1000 rpm, 10 s then 5000 rpm, 20 s. The samples were immediately baked on a hotplate at 150 °C for



10 min. Two layers of ZnO were coated repeating this process, followed by a final anneal at 450 °C for 2–3 h. After returning to RT, this layer was pattered by photolithography and etched with a 5% v/v solution of acetic acid (glacial, ≥99%, Sigma Aldrich UK) to create the active layer islands. The S–D contacts were then aligned (Mask Aligner Suss MA 1006) on top of the ZnO islands and patterned by photolithography, prior to thermally evaporating (Moorfiled Nanotechnology Thermal Evaporator) a 3 nm thin barrier layer of MoO₃ nanoparticles (Sigma Aldrich UK). Next, the metal contacts 10 nm Cr and 100 nm Au were deposited through electron beam deposition (Univex 5009 Electron Beam Evaporator), followed by lift-off of the photoresist in acetone, to realize the completed transistor devices.

Polycrystalline Silicon Transistor Fabrication: Self-aligned bottom gate top contact LTPS SGTs were fabricated on glass substrates in multiple batches at Philips MiPlaza in 2006–2009 (the full process has been reported in Ref. [20]). Starting with definition of a Cr gate, consecutive 100 nm gate dielectrics of SiN_x and SiO₂ were deposited by PECVD, followed by 40 nm a-Si:H. After definition and doping of the high n-type drain region, polysilicon islands were formed with excimer laser and dry etching. A 120 nm SiO₂ field plate insulator was then deposited and source contact windows were opened, through which 5 keV ion implantation of either 5×10^{12} cm⁻² P (device thus far unpublished and denoted LTPS(P)) or 1×10^{13} cm⁻² BF₂ device first reported in Ref. [9] and identified as LTPS(BF₂) was performed to modify the source energy barrier height. Cr was deposited as the contact metal and Ti/Al used for the field plate structure.

Acknowledgements

R.A.S. thanks J. M. Shannon, N. D. Young, and M. J. Trainor for the design and fabrication of polysilicon devices. Partial support for this project was provided by the Engineering and Physical Sciences Research Council, UK through grants EP/R028559/1 and EP/V002759/1.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

contact resistance, energy barrier, flat saturation, high gain, thin-film transistor $% \left({{\left[{{{\rm{s}}_{\rm{s}}} \right]}_{\rm{s}}} \right)$

Received: October 11, 2021 Revised: October 31, 2021 Published online: December 15, 2021

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