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Subthreshold Swing of 59 mV decade^{-1} in Nanoscale Flexible Ultralow-Voltage Organic Transistors

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Organic thin-film transistors (TFTs) that provide subthreshold swings near the theoretical limit together with large on/off current ratios at very low operating voltages require high-capacitance gate dielectrics with a vanishingly small defect density. A promising approach to the fabrication of such dielectrics at temperatures sufficiently low to allow TFT fabrication on polymeric substrates are hybrid dielectrics consisting of a thin metal oxide layer in combination with a molecular self-assembled monolayer (SAM). Here, the electrical and surface properties of titanium oxide produced by the plasma-assisted oxidation of the surface of vacuum-deposited titanium gate electrodes and its use as the first component of a hybrid TiO_x/SAM gate dielectric in flexible organic TFTs are investigated. These transistors have a gate-dielectric capacitance of about 1 µF cm^{-2}, a subthreshold swing of 59 mV decade^{-1} (within measurement error of the physical limit at room temperature) for a wide range of channel lengths as small as 0.7 µm, and an on/off current ratio of 10^7 for a gate-source-voltage range of 1 V.

1. Introduction

Organic thin-film transistors (TFTs) can typically be fabricated at substantially lower temperatures than transistors based on inorganic semiconductors, making them potentially useful for the realization of flexible active-matrix displays, wearable sensors and low-power integrated circuits.[1–4] A key component of organic TFTs for such advanced technologies is the gate dielectric.[5] Among the prerequisites enabling low-voltage TFT operation is a large unit-area gate-dielectric capacitance, which can be achieved by implementing either ultrathin and/or high-permittivity dielectrics.[6–8] The gate dielectric is also critical in determining the threshold voltage, the subthreshold swing and the bias-stress stability of the TFTs.[9–12] For organic TFTs fabricated in the inverted (bottom-gate) device architecture, the surface properties of the gate dielectric have a pronounced influence on the growth and the quality of the organic-semiconductor film.[13–15] Overall, the gate dielectric has essential and far-reaching impact on the performance and stability of field-effect transistors in general and organic TFTs in particular.

A possible limitation of aluminum oxide as the gate oxide in field-effect transistors is its relatively small permittivity, which limits the unit-area capacitance of low-leakage hybrid AlO_x/SAM dielectrics to about 0.7 µF cm^{-2}.[24] Majewski et al. and Jinno et al. thus introduced titanium oxide, grown by anodic oxidation on the surface of titanium gate electrodes, and demonstrated hybrid TiO_x/SAM dielectrics with a unit-area capacitance close to 1 µF cm^{-2} and organic TFTs capable of operating in the saturation regime with gate-source and drain-source voltages of just 1 V.[25–27] This represents an important achievement, as it fulfills a critical requirement for low-voltage electronic systems that are to be powered by small batteries, solar cells or energy-harvesting devices, or which are to be in direct contact with human tissue.[28–30] A challenge that arises from using titanium oxide is its smaller bandgap that makes it more difficult to achieve small gate currents, large on/off current ratios and small subthreshold swings. In the TFTs reported by Majewski et al. and Jinno et al., the gate currents exceeded 10^{-11} A, the on/off current ratios were no greater than 10^5, and the subthreshold swings were above 100 mV decade^{-1}.

Here we show that the formation of ultrathin titanium oxide dielectrics by plasma-assisted oxidation, rather than anodization, leads to ultralow-voltage organic TFTs on plastic substrates that set a number of organic-TFT-performance records, including a subthreshold swing of 59 mV decade^{-1} (i.e., close to the physical limit at room temperature) for TFTs with channel lengths as small as 0.7 µm and an on/off current ratio of 10^7 for a gate-source-voltage range of 1 V. In addition, we also fabricated unipolar inverters that display a small-signal gain of 1900 in combination with a noise

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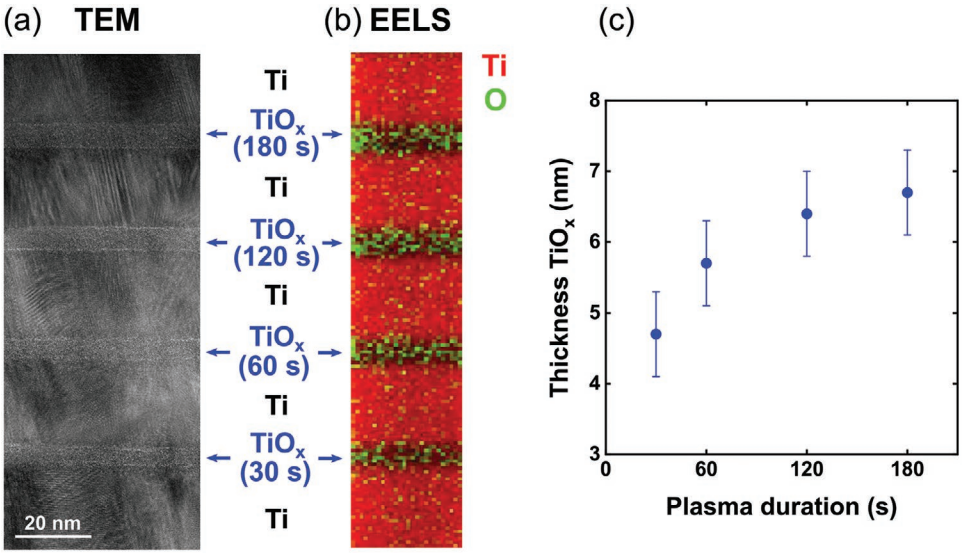

Figure 1. a) Cross-sectional transmission electron microscopy (TEM) image of titanium oxide films (TiO_x) produced sequentially by the plasma-assisted surface oxidation of vacuum-deposited titanium films. Surface oxidation was performed using a plasma power of 200 W and plasma durations of 30, 60, 120, and 180 s. b) Elemental mapping of titanium and oxygen obtained from the Ti-$L_{2,3}$ and O-K edges of the electron energy loss spectroscopy (EELS) spectra. c) Thickness of the TiO_x films determined from the TEM image plotted as a function of the plasma duration.

margin of 79% of half the supply voltage at a supply voltage of 1 V. This is the best combination of small-signal gain and noise margin reported to date for organic-TFT-based unipolar inverters operating with supply voltages of less than 20 V.

2. Results and Discussion

2.1. Thickness of Plasma-Grown TiO_x Films

Figure 1a shows a cross-sectional transmission electron microscopy (TEM) image of a specimen prepared on a silicon substrate by depositing a 25-nm-thick film of titanium by thermal evaporation in vacuum, followed by exposing the titanium surface to a radio-frequency-generated oxygen plasma to form a thin layer of titanium oxide (TiO_x). These two process steps were repeated four times on the same specimen, each time using a different duration for the plasma-oxidation process (30, 60, 120, and 180 s). To be able to unambiguously identify and distinguish the metal and oxide layers in the cross-sectional image, electron energy loss spectroscopy (EELS) was performed. The elemental distribution was obtained by mapping the Ti-$L_{2,3}$ and O-K edges of the recorded spectra (see Figure 1b).

The TEM analysis indicates that the thickness of the plasma-grown titanium oxide films ranges from 4.7 nm for the shortest plasma duration (30 s) to 6.7 nm for the longest duration (180 s). Figure 1c shows the experimentally determined relation between the plasma duration and the thickness of the TiO_x films. The range of TiO_x thicknesses obtained here is similar to the range of thicknesses reported previously for plasma-grown AlO_x films.[24]

2.2. Electrical and Surface Properties of Plasma-Grown TiO_x and Hybrid TiO_x/SAM Dielectrics

To investigate the electrical properties of plasma-grown TiO_x and hybrid TiO_x/SAM dielectrics, we fabricated metal-insulator-metal capacitors on flexible polyethylene naphthalate (PEN) substrates. For the bottom electrode, titanium with a thickness of 25 nm was deposited by thermal evaporation in vacuum. The TiO_x films were obtained by plasma-assisted oxidation of the titanium surface with plasma durations of 30, 60, 120, or 180 s. For the hybrid TiO_x/SAM dielectrics, a monolayer of *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid was allowed to self-assemble from solution on the TiO_x surface.[31] For the top electrode, gold with a thickness of 30 nm was deposited by vacuum evaporation. The electrodes were patterned using silicon stencil masks.[32] In **Figure 2**a,b, schematic cross sections of capacitors with a bare-TiO_x dielectric or a hybrid TiO_x/SAM dielectric are shown.

An important prerequisite for minimizing the charge leakage through ultrathin gate dielectrics in TFTs fabricated in the inverted (bottom-gate) device architecture is a small surface roughness of the gate electrodes. Figure S1 (Supporting Information) shows atomic force microscopy (AFM) images of a bare PEN substrate and of nominally 25-nm-thick titanium and aluminum films deposited by thermal evaporation onto PEN. Analysis of the AFM images indicates that all three surfaces (PEN, Ti on PEN, Al on PEN) have essentially the same root-mean-square surface roughness of (1.6 ± 0.1) nm, confirming that the surface roughness of vacuum-deposited titanium is just as small as that of vacuum-deposited aluminum and that both metals cover the PEN surface in a conformal manner.

Obtaining a favorable thin-film morphology of the vacuum-deposited small-molecule organic semiconductor greatly benefits from a small surface energy of the underlying gate dielectric. For hybrid TiO_x/SAM dielectrics based on plasma-grown titanium oxide, we have measured water contact angles of (109 ± 2)° with *n*-tetradecylphosphonic acid SAMs and (108 ± 2)° with *n*-octadecylphosphonic acid SAMs, essentially identical to hybrid AlO_x/SAM dielectrics[33] and confirming that plasma-grown, SAM-functionalized gate oxides provide very small

surface energies. While gate dielectrics with small surface energies are beneficial for TFTs based on vacuum-deposited organic semiconductors, they often present problems if the semiconductor deposition is to be performed from solution, due to poor wetting of the semiconductor solution on low-energy surfaces. However, Wöbkenberg et al. previously demonstrated that the solution-deposition of organic semiconductors on hybrid oxide/SAM gate dielectrics with very low surface energy is in fact possible, provided the use of specifically tailored organic semiconductors with compatible surface properties.[34]

The current-voltage characteristics of the metal-insulator-metal capacitors were measured to analyze the influence of the plasma duration on the leakage-current density through the dielectrics. For the bare-TiO_x dielectrics, the leakage-current density is smaller for longer plasma durations, which is consistent with the growth of thicker TiO_x films with longer plasma duration, as confirmed by the TEM investigation. Nevertheless, as seen in Figure 2c, bare-TiO_x dielectrics exhibit overall high leakage-current densities, indicating poor insulating properties. Due to the small bandgap of about 3.5 eV, thermionic emission is a serious concern for bare-TiO_x dielectrics.[35,36]

However, when the TiO_x films are complemented by an alkylphosphonic acid SAM, the leakage-current densities are significantly smaller, i.e., below 10^{-5} A cm^{-2} at a voltage of –1 V for the *n*-tetradecylphosphonic acid SAM and below 10^{-6} A cm^{-2} at a voltage of –1 V for the *n*-octadecylphosphonic acid SAM and for plasma durations of at least 120 s (see Figure 2d,e). These leakage-current densities are not significantly larger than those measured previously in hybrid AlO_x/SAM dielectrics.[24]

In Figure 2f–h, the measured unit-area capacitance is shown for different plasma durations as a function of the measurement frequency. The unit-area capacitance of the bare-TiO_x dielectrics ranges from 1.1 to 3.0 μF cm^{-2} with a clear dependence on the plasma duration. The additional contribution of the SAM decreases the capacitance of the hybrid TiO_x/SAM dielectric and leads to a much less pronounced dependence on the plasma duration (1.1 to 1.4 μF cm^{-2} for the n-tetradecylphosphonic acid SAM; 0.7 to 0.8 μF cm^{-2} for the n-octadecylphosphonic acid SAM).

Figure 2j shows the measured unit-area capacitance of the bare-TiO_x dielectrics plotted as a function of the inverse of the TiO_x thickness, as determined by TEM. By fitting the theoretical relation between the unit-area oxide capacitance C_{ox} and the oxide thickness t_{ox}:

$$C_{ox} = \varepsilon_0 \, \varepsilon_{ox} \frac{1}{t_{ox}} \quad (1)$$

where ε_0 is the vacuum permittivity, a value for the permittivity of the plasma-grown titanium oxide of $\varepsilon_{ox} = 14 \pm 1$ is obtained. (See Figure S2 (Supporting Information) for details on the error calculation.) This value falls into the range of permittivities reported for titanium oxide in literature.[34,37–41]

In summary, the results of the measurements of the electrical properties of the plasma-grown TiO_x and hybrid TiO_x/SAM dielectrics show that a plasma duration of 120 s is sufficient to minimize the charge leakage through hybrid TiO_x/SAM dielectrics. Taking this as a prerequisite, the unit-area capacitance of the hybrid TiO_x/SAM dielectric is 1.1 μF cm^{-2} for the *n*-tetradecylphosphonic acid SAM and 0.7 μF cm^{-2} for the *n*-octadecylphosphonic acid SAM. Together with the results of the surface-roughness and contact-angle measurements, the hybrid TiO_x/SAM dielectric meets the general requirements for low-voltage organic TFTs.

2.3. Organic TFTs

Organic TFTs with a hybrid TiO_x/SAM gate dielectric were fabricated on flexible PEN substrates in the inverted coplanar (bottom-gate, bottom-contact) device architecture without encapsulation. For the gate electrodes, a 25-nm-thick film of titanium was deposited by thermal evaporation in vacuum. The titanium surface was exposed to an oxygen plasma, and the substrates were then immersed into a solution of *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid. For the source and drain contacts, gold with a thickness of 30 nm was deposited and functionalized with a monolayer pentafluorobenzenethiol (PFBT) to minimize the contact resistance.[21,22] As the semiconductor, either 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT) or 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT) was deposited by thermal sublimation in vacuum.[6,10,42] The metals and the organic-semiconductor layers were patterned using silicon stencil masks.[32] The highest process temperature is the temperature at which the substrate is held during the deposition of the organic semiconductor, i.e., 100°C for the DPh-BTBT TFTs and 90°C for the DPh-DNTT TFTs. All electrical measurements were performed in ambient air at room temperature (293 K).

DPh-BTBT, whose chemical structure is shown as part of **Figure 3**a, is a commercially available small-molecule semiconductor developed by Kazuo Takimiya.[43] DPh-BTBT TFTs fabricated with a hybrid AlO_x/SAM gate dielectric and a fluoroalkylphosphonic acid SAM have previously shown a turn-on voltage of exactly 0 V,[10] which can be of great value for the efficient design of low-voltage, low-power digital integrated circuits.[6]

Figure 3a,b shows a schematic cross section of a TFT with a hybrid TiO_x/SAM dielectric and a photograph of a PEN substrate with arrays of TFTs and circuits. A scanning electron microscopy (SEM) image of a DPh-BTBT TFT with a channel length of 0.7 μm and the measured transfer and output characteristics of this TFT are shown in Figure 3c–e. The small channel length is helpful in achieving a large channel-width-normalized transconductance of 0.6 S m^{-1} at a gate-source voltage of –1 V. Owing to the exceptional combination of large unit-area gate-dielectric capacitance and insignificant gate leakage, an on/off current ratio of 10^7 is obtained for the gate-source-voltage range from 0 to –1 V. To our knowledge, these are the largest width-normalized transconductance and the largest on/off current ratio reported to date for flexible organic TFTs for a gate-source-voltage range of 1 V or less.[6]

The subthreshold swing of the DPh-BTBT TFTs is determined to be (59 ± 1) mV decade^{-1} for a drain-source voltage of –0.1 V and (62 ± 2) mV decade^{-1} for a drain-source voltage of –0.7 V (see Figure 3f–h). To our knowledge, this is the first time that a subthreshold swing below 66 mV decade^{-1} is reported for a submicron-channel-length organic transistor.[22,47,48] The

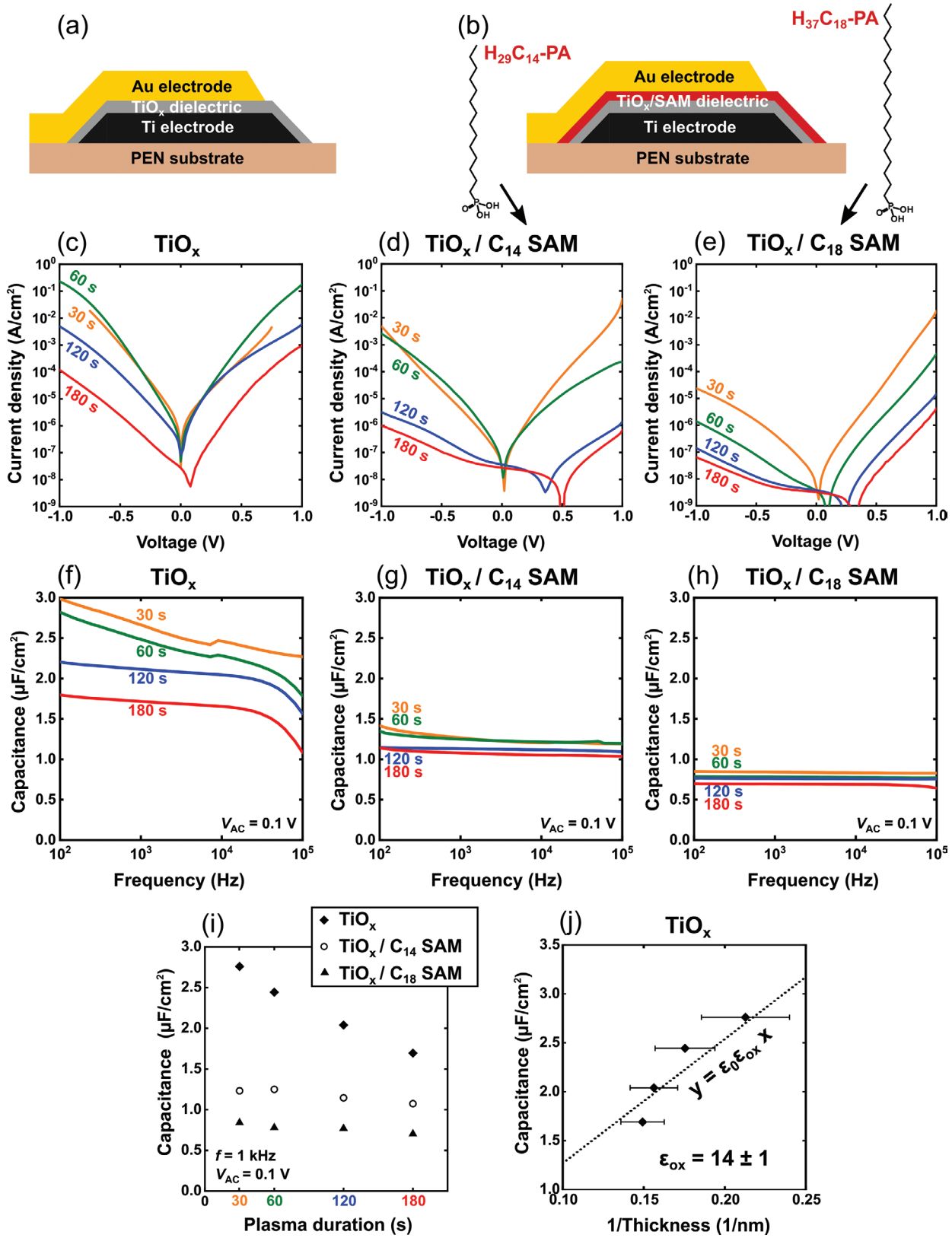

Figure 2. Schematic cross sections of metal-insulator-metal capacitors based on a) bare plasma-grown TiO_x as the dielectric and b) a hybrid dielectric consisting of plasma-grown TiO_x and an *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid self-assembled monolayer (SAM). c–e) Measured leakage current density and f–i) unit-area capacitance. j) Unit-area capacitance of capacitors based on bare plasma-grown TiO_x plotted as a function of the inverse of the TiO_x thickness, as determined by TEM, to calculate the relative permittivity of the plasma-grown titanium oxide.

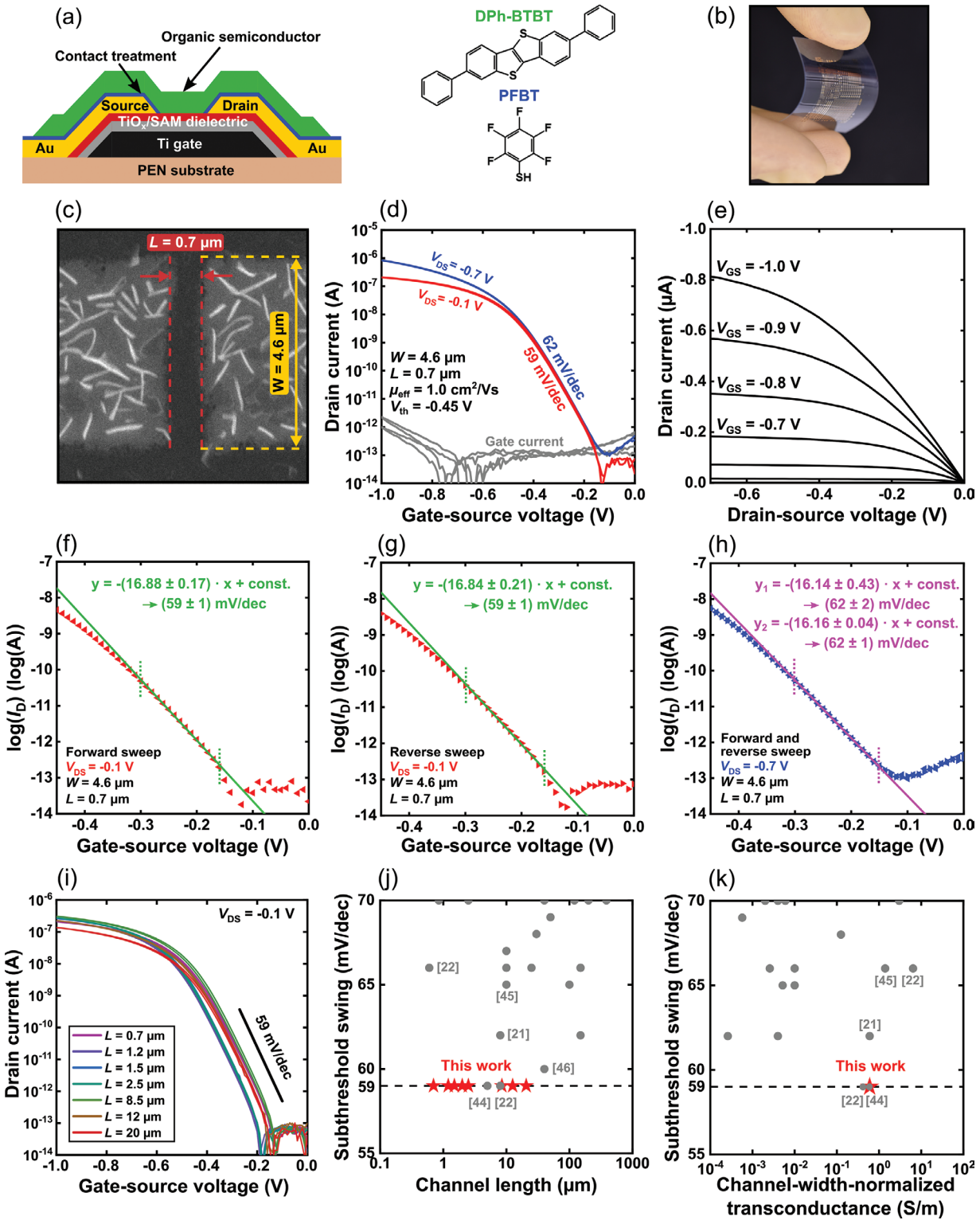

Figure 3. a) Schematic cross section of organic thin-film transistors (TFT) with a hybrid TiO_x/SAM gate dielectric, and molecular structures of the organic semiconductor 2,7-diphenyl-[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT) and of the molecule pentafluorobenzenethiol (PFBT) employed to functionalize the gold source and drain contacts with a chemisorbed monolayer to minimize the contact resistance. b) Photograph of a flexible PEN substrate with arrays of organic TFTs and circuits. c) Scanning electron microscopy (SEM) image of a flexible DPh-BTBT TFT with a channel length of 0.7 µm. d) Measured transfer and e) output characteristics of a flexible DPh-BTBT TFT having a channel length of 0.7 µm. f–h) Extraction of the subthreshold swing from the transfer characteristics. i) Measured transfer characteristics of flexible DPh-BTBT TFTs with a Ti/TiO_x/SAM gate stack and channel lengths ranging from 0.7 to 20 µm. j) Literature summary of organic TFTs with subthreshold swings of 70 mV decade^{-1} or less, plotted versus the channel length, and k) plotted versus the channel-width-normalized transconductance of the transistors.

subthreshold swing of 59 mV decade^{-1} was measured here in flexible TFTs with channel lengths ranging from 0.7 to 20 μm (see Figure 3i,j).

For the temperature at which these measurements were performed (T = 293 K), the subthreshold swing of (59 ± 1) mV decade^{-1} is within the measurement error of the theoretical minimum of 58.1 mV decade^{-1}, given as $\ln(10)k_BT/q$, where k_B is the Boltzmann constant and q is the elementary charge.[49] This confirms that it is possible to fabricate nanoscale organic TFTs with minimum subthreshold swing on flexible substrates, provided an optimized combination of materials and techniques for film formation and patterning is employed for all transistor components, including high-fidelity lithography and a native interface between the gate metal and the gate oxide that is characterized by a vanishingly small defect density.

One drawback of DPh-BTBT TFTs is their relatively large contact resistance. Using the transmission line method (TLM) in the linear regime of operation, we determined a channel-width-normalized contact resistance of (142 ± 37) Ω cm for flexible DPh-BTBT TFTs with a hybrid TiO_x/SAM dielectric (see **Figure 4**a–c). Notably smaller contact resistances can be expected by replacing DPh-BTBT with DPh-DNTT (chemical structure shown in **Figure 5**a), which was also developed by Kazuo Takimiya[50] and for which a contact resistance of 29 Ω cm (also determined by TLM in the linear regime of operation) was recently obtained in flexible TFTs with a hybrid AlO_x/SAM gate dielectric.[21]

Figure 5b,c shows the measured transfer and output characteristics of a flexible DPh-DNTT TFT with a hybrid TiO_x/SAM gate dielectric having a channel length of 2.4 μm. The DPh-DNTT TFTs have an on/off current ratio of 10^7 within a gate-source-voltage range of 1 V (similar to the DPh-BTBT TFTs) and a subthreshold swing of (63 ± 1) mV dec^{-1} for a drain-source voltage of –0.1 V and (66 ± 1) mV dec^{-1} for a drain-source voltage of –0.6 V (see Figure 5d).

To probe the bias-stress stability of these TFTs, gate-source and drain-source voltages of –0.6 V were applied continuously for a duration of 72 h in ambient air. In Figure 5e, the normalized drain current is plotted as a function of bias-stress duration, and Figure 5f shows the transfer characteristics of the TFT measured before and after the bias-stress test. The 72 h bias-stress test caused a threshold-voltage shift of –0.01 V and a drain-current reduction of 6%. Considering that the TFTs were fabricated on a plastic substrate without encapsulation and that the bias stress was applied in ambient air and for a duration of three days, the bias-stress stability reported here is on par with the best results reported in literature (see **Table 1**). This further confirms the excellent quality of hybrid TiO_x/SAM gate dielectrics based on plasma-grown titanium oxide.[51]

Figure 6 shows the transfer characteristics of DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack in comparison to those of DPh-DNTT TFTs with an Al/AlO_x/SAM gate stack. The only noteworthy difference between the transfer curves is the threshold voltage, which has values of –0.07 V for the TFTs with the Ti/TiO_x/SAM gate stack and –0.53 V for the TFTs with the Al/AlO_x/SAM gate stack. The threshold voltage of organic TFTs can be approximated as:[56]

$$V_{th} = \frac{Q_{sc} - Q_{diel}}{C_{diel}} + \Phi_{ms} \quad (2)$$

where Q_{sc} is the density of free charge carriers in the semiconductor at equilibrium (i.e., no voltages applied), Q_{diel} is the density of charges in the gate dielectric or at the semiconductor-dielectric interface, C_{diel} is the unit-area gate-dielectric capacitance and Φ_{ms} is the difference between the workfunction of the metal and the semiconductor. The difference between the workfunctions of titanium (4.33 eV)[57] and aluminum (4.23 to 4.32 eV)[58,59] is too small to explain the observed difference between the threshold voltages in Figure 6 (0.46 V). It thus appears that there is a significant difference in the density of charges in the semiconductor (Q_{sc}) and/or in the gate dielectric and/or at the semiconductor-dielectric interface (Q_{diel}) that is responsible for the observed difference in the threshold voltages of the TFTs. It will certainly be useful to investigate the exact origin(s) and location(s) of these charges and the question how these relate to the materials properties of plasma-grown titanium oxide and aluminum oxide, but such investigations are beyond the scope of the present study.

In addition to a steep subthreshold swing, a large on/off current ratio and good bias-stress stability, organic TFTs also need to have a small contact resistance. Figure 4d–i shows results of a TLM analysis of flexible DPh-DNTT TFTs with the two different gate stacks (Ti/TiO_x/SAM and Al/AlO_x/SAM). The width-normalized contact resistance at the highest gate overdrive voltage (difference between gate-source voltage and threshold voltage) is (15 ± 5) Ω cm for the TFTs with the titanium gates (long-term stability of the contact resistance shown in Figure S3: Supporting Information) and (12 ± 2) Ω cm for the TFTs with the aluminum gates. These are the smallest contact resistances reported to date for organic TFTs in the linear regime of operation, aside from the contact resistances of 1 Ω cm reported by Braga et al. and 3 Ω cm reported by Lenz et al. for an electrolyte-gated polymer TFTs in which the contact resistance benefits greatly from the extremely large charge-carrier density induced by the electrolyte[60,61] For DPh-DNTT TFTs operated in the saturation regime, Borchert et al. recently reported a contact resistance of 10 Ω cm extracted from scattering-parameter measurements.[22]

The intrinsic channel mobility extracted from the TLM analysis in Figure 4 is about 30% smaller in the DPh-DNTT TFTs with the titanium gates (3.0 cm^2 V^{-1} s^{-1}) than in the DPh-DNTT TFTs with the aluminum gates (4.6 cm^2 V^{-1} s^{-1}). This difference in intrinsic channel mobility is possibly related to the formation of Fröhlich polarons,[14,62] which is known to be more prominent for a larger gate-oxide permittivity (TiO_x: 14 ± 1; AlO_x: 8.0 ± 0.2).[24] The compromise between the gate-dielectric permittivity and the charge-carrier mobility is a general problem for organic TFTs, and the smaller mobility we have found here for the TFTs with the Ti/TiO_x/SAM gate stack is an obvious drawback in comparison to TFTs with an Al/AlO_x/SAM gate stack.

Also shown in Figure 4 is the analysis of the contact resistance according to the formulation developed by Luan and Neudeck, in which the contact resistance R_CW is modeled as the sum of two terms, one that decreases with increasing gate-source voltage and one that represents a minimum contact resistance $R_{C,0}W$ that is independent of the gate-source voltage:[63]

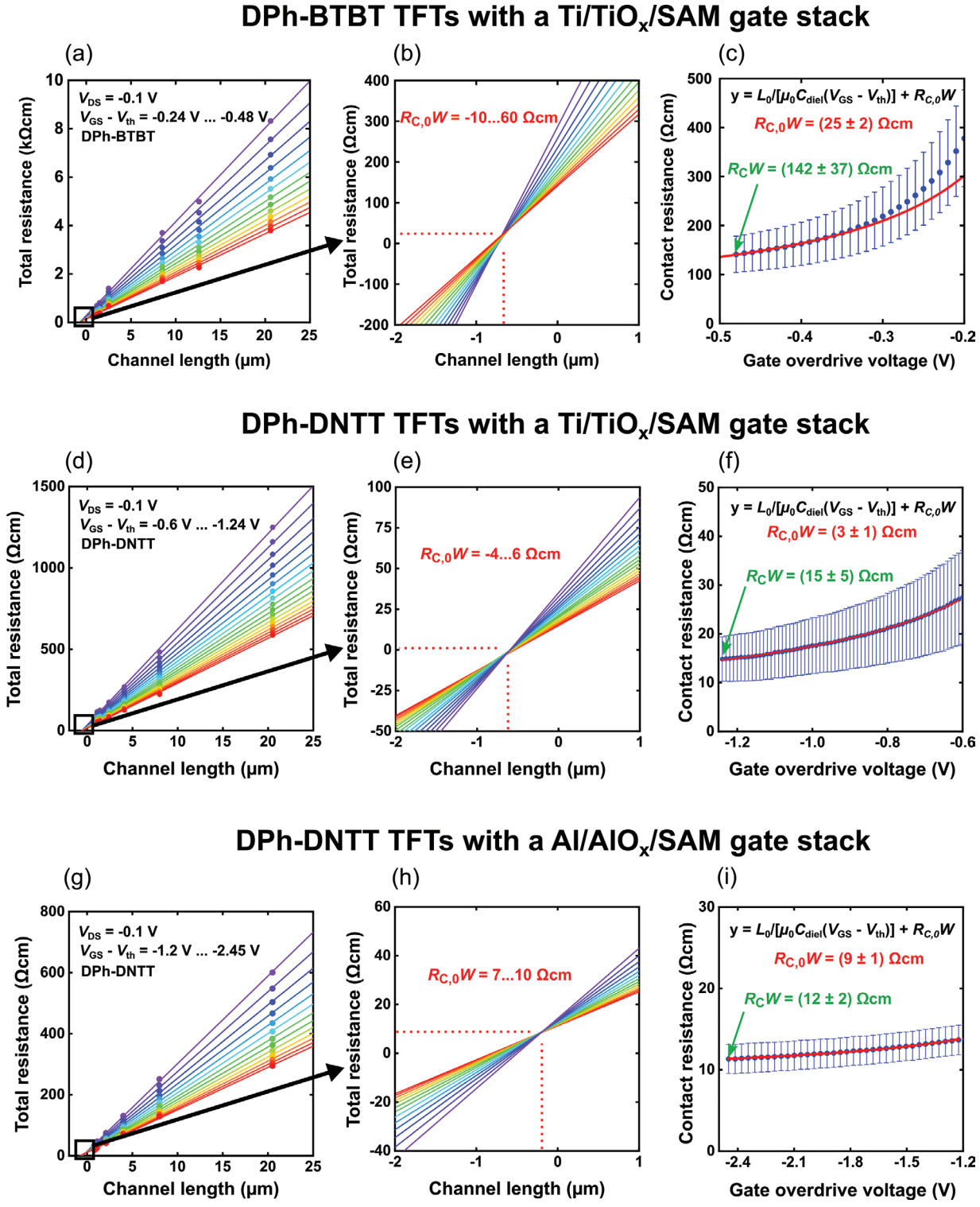

Figure 4. a) Transmission line method (TLM) analysis of flexible DPh-BTBT TFTs with a Ti/TiO_x/SAM gate stack. b) The gate-source-voltage-independent minimum contact resistance $R_{C,0}W$ can be estimated from the intercept of the individual fit lines in the plot of the total device resistance RW versus the channel length L. c) Channel-width-normalized contact resistance plotted as a function of the gate overdrive voltage. For the largest gate overdrive voltage (V_{GS}-V_{th} = –0.48 V), a width-normalized contact resistance R_CW of (142 ± 37) Ω cm is extracted. Fitting Equation (1) to the R_CW = f(V_{GS}-V_{th}) data yields a value for $R_{C,0}W$ of (25 ± 2) Ω cm. d) TLM analysis of flexible DPh-DNTT TFTs with an Ti/TiO_x/SAM gate stack. e) Extrapolation of the fit lines to estimate $R_{C,0}W$. f) Width-normalized contact resistance plotted as a function of the gate overdrive voltage, yielding R_CW = (15 ± 5) Ω cm for the largest gate overdrive voltage (V_{GS}-V_{th} = –1.24 V) and $R_{C,0}W$ = (3 ± 1) Ω cm. g) TLM analysis of flexible DPh-DNTT TFTs with an Al/AlO_x/SAM gate stack. h) Extrapolation of the fit lines. i) Width-normalized contact resistance plotted as a function of the gate overdrive voltage, yielding R_CW = (12 ± 2) Ω cm for the largest gate overdrive voltage (V_{GS}-V_{th} = –2.45 V) and $R_{C,0}W$ = (9 ± 1) Ω cm.

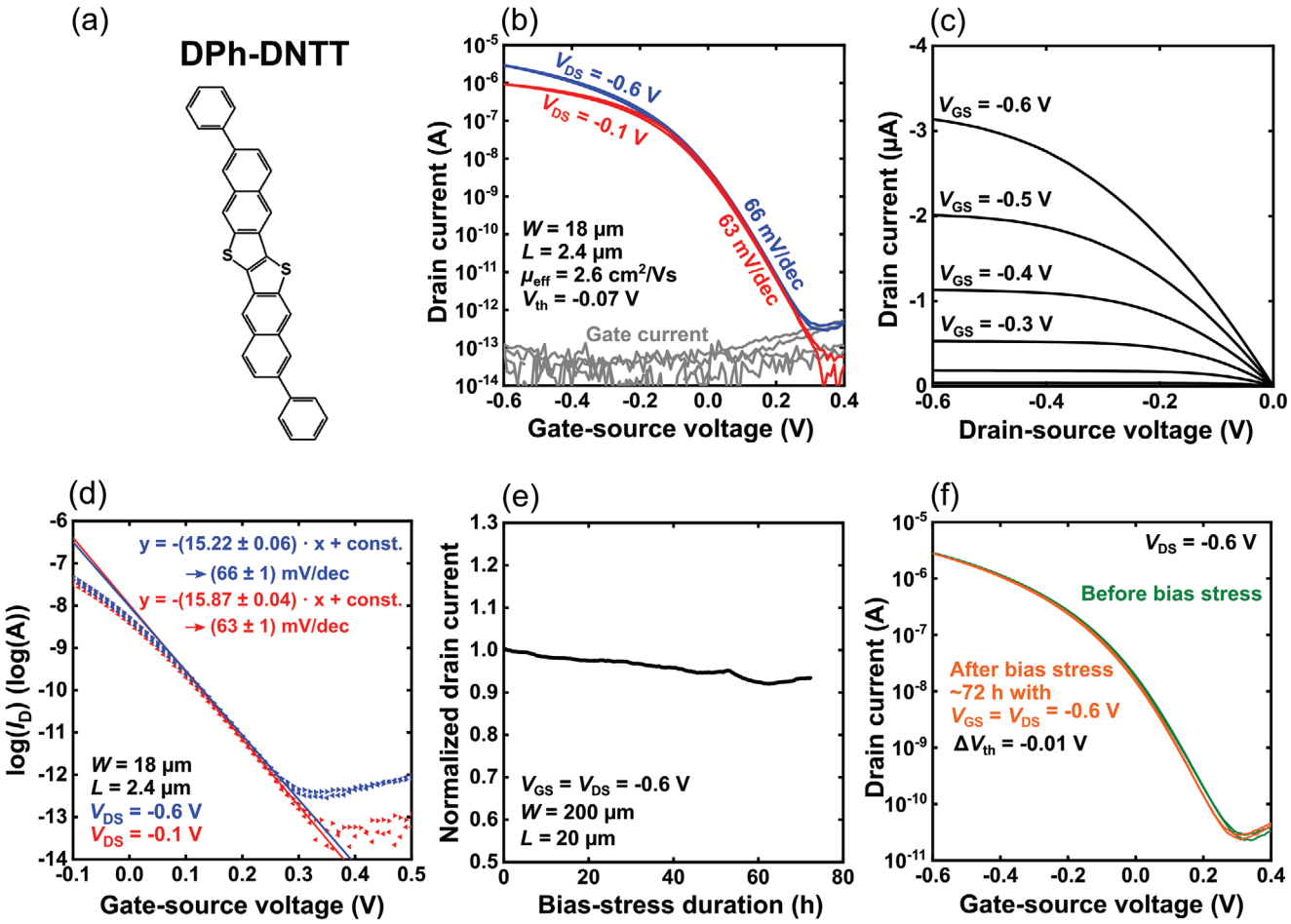

Figure 5. a) Molecular structure of the organic semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT). b) Measured transfer and c) output characteristics of a flexible DPh-DNTT TFT with a hybrid TiO_x/SAM gate dielectric having a channel length of 2.4 µm. d) Extraction of the subthreshold swing from the transfer characteristics. e) Evolution of the drain current of a flexible DPh-DNTT TFT with a hybrid TiO_x/SAM gate dielectric during a bias stress. f) Transfer characteristics of the same TFT measured before and after bias stress for a duration of 72 h.

$$R_C W = \frac{L_0}{\mu_0 C_{diel}(V_{GS} - V_{th})} + R_{C,0} W \quad (3)$$

where μ_0 is the intrinsic channel mobility, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, W is the channel width, and L_0 is a characteristic contact length. The values of L_0 and $R_{C,0}W$ can be extracted from the intercept of the individual fit lines in the plot of the total device resistance RW versus the channel length L (see Figure 4e,h), and alternatively by fitting the above equation to the plot of the contact resistance $R_C W$ versus the gate overdrive voltage V_{GS}-V_{th} (see Figure 4f,i). Values for $R_{C,0}W$ of (3 ± 1) Ω cm and (9 ± 1) Ω cm were found

Table 1. Comparison of the bias-stress stability of the flexible low-voltage DPh-DNTT TFTs in Figure 5e,f with the bias-stress stability of organic TFTs reported by Kalb et al. in 2007, by Jia et al. in 2018, and by Iqbal et al. in 2021. The parameter N_{trap}/N_{init} was calculated using Equation (2) in ref. [52].

Ref.	C_{diel} [nF cm^{-2}]	V_{GS} [V]	$C_{diel}(V_{GS}$-$V_{th})$ [C cm^{-2}]	Substrate	Measurement ambient	Encapsulation	Semiconductor	Bias-stress duration [h]	ΔV_{th} [V]	N_{trap}/N_{init} [%]
[53]	3.5	−70	$2.5 \cdot 10^{-7}$	Glass	Helium	None	Single-crystalline Rubrene	2	−0.18	0.3
[54]	40.8	−10	$3.3 \cdot 10^{-7}$	Glass	Nitrogen	None	Solution-deposited TIPS- pentacene/PTAA	163	−0.04	0.5
[55]	17.3	−35	$4.3 \cdot 10^{-7}$	Si wafer	Air	Parylene N	Solution-deposited IDT-BT	8	+0.1	0.4
This work	1100	−0.6	$5.8 \cdot 10^{-7}$	Flexible PEN	Air	None	Vacuum-deposited DPh-DNTT	72	−0.01	1.8

Table 2. Summary of the parameters of the TFTs with the Ti/TiO_x/SAM gate stack from Figure 3d, of the DPh-DNTT TFTs with the Ti/TiO_x/SAM gate stack from Figure 5b, and of the DPh-DNTT TFTs with the Al/AlO_x/SAM gate stack from Figure 6.

Substrate	Gate stack	Semi-conductor	L [μm]	S [mV dec^{-1}]	on/off ratio	V_{th} [V]	$R_C W$ [Ω cm]	$R_{C,0} W$ [Ω cm]	μ_0 [cm^2 V^{-1} s^{-1}]	g_m/W [S m^{-1}]
PEN	Ti/TiO_x/SAM	DPh-BTBT	0.7	59 mV dec^{-1}	10^7	−0.45	142 ± 37	25 ± 2	1.8	0.6
PEN	Ti/TiO_x/SAM	DPh-DNTT	2.4	63 mV dec^{-1}	10^7	−0.07	15 ± 5	3 ± 1	3.0	0.6
PEN	Al/AlO_x/SAM	DPh-DNTT	2.4	71 mV dec^{-1}	10^7	−0.53	12 ± 2	9 ± 1	4.6	0.5

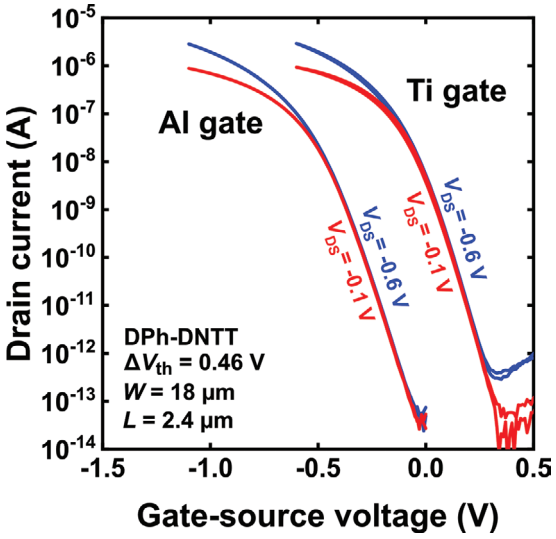

Figure 6. Measured transfer characteristics of flexible DPh-DNTT TFTs with an Al/AlO_x/SAM gate stack (left) and a Ti/TiO_x/SAM gate stack (right). The TFTs with the Al/AlO_x/SAM gate stack have a negative turn-on voltage, while the TFTs with the Ti/TiO_x/SAM gate stack have a positive turn-on voltage. The difference between the threshold voltages is 0.46 V.

for the DPh-DNTT TFTs with the Ti/TiO_x/SAM gate stack and the Al/AlO_x/SAM gate stack, respectively. These results suggest that further optimization of the materials and/or device architecture might lead to a contact resistance of about 1 Ω cm or perhaps even below 1 Ω cm in organic TFTs with ultrathin, high-capacitance gate dielectrics.

Table 2 summarizes the parameters of the DPh-BTBT TFTs with the Ti/TiO_x/SAM gate stack from Figure 3d, of the DPh-DNTT TFTs with the Ti/TiO_x/SAM gate stack from Figure 5b, and of the DPh-DNTT TFTs with the Al/AlO_x/SAM gate stack from **Figure 6**.

2.4. Zero-V_{GS} Inverters Based on a Normally-On Load and a Normally-Off Drive TFT

The fact that DPh-DNTT TFTs have a positive turn-on voltage when fabricated with a Ti/TiO_x/SAM gate stack but a negative turn-on voltage when fabricated with an Al/AlO_x/SAM gate stack (see Figure 6) can be exploited for the fabrication of zero-V_{GS} inverters with a normally-on ("depletion-mode") load and a normally-off ("enhancement-mode") drive transistor. The circuit schematic of the zero-V_{GS} inverter is shown in **Figure 7**a. There are numerous reports of organic-TFT-based zero-V_{GS} inverters,[28,30,44,64] but in most of these reports, the inverters were based on two normally-off or two normally-on transistors. However, the optimum design of zero-V_{GS} inverters utilizes a normally-off drive transistor to provide a switching voltage close to half the supply voltage (and thus noise margins close to 100% of half the supply voltage) and a normally-on load transistor to facilitate rapid discharging of the output node when the drive transistor is non-conducting.[65–68] Properly designed zero-V_{GS} inverters are advantageous in comparison to other unipolar inverter styles, as they provide a larger small-signal gain and larger noise margins than diode-load and biased-load inverters, and a smaller TFT count and shorter signal delays than pseudo-CMOS inverters.[69,70] We fabricated zero-V_{GS} inverters with a

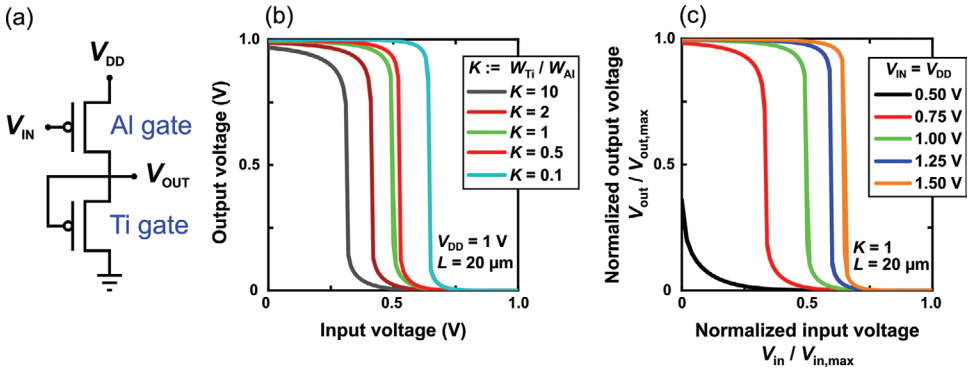

Figure 7. a) Circuit schematic of a zero-V_{GS} inverter, here based on a normally-on load TFT (Ti/TiO_x/SAM gate stack) and a normally-off drive TFT (Al/AlO_x/SAM gate stack). Both TFTs utilize the same organic semiconductor (DPh-DNTT). b) Measured transfer characteristics of zero-V_{GS} inverters with different channel-width ratios ($K = W_{load}/W_{drive}$). c) Transfer characteristics of a zero-V_{GS} inverter with a channel-width ratio $K = 1$ measured for supply voltages V_{DD} ranging from 0.5 to 1.5 V.

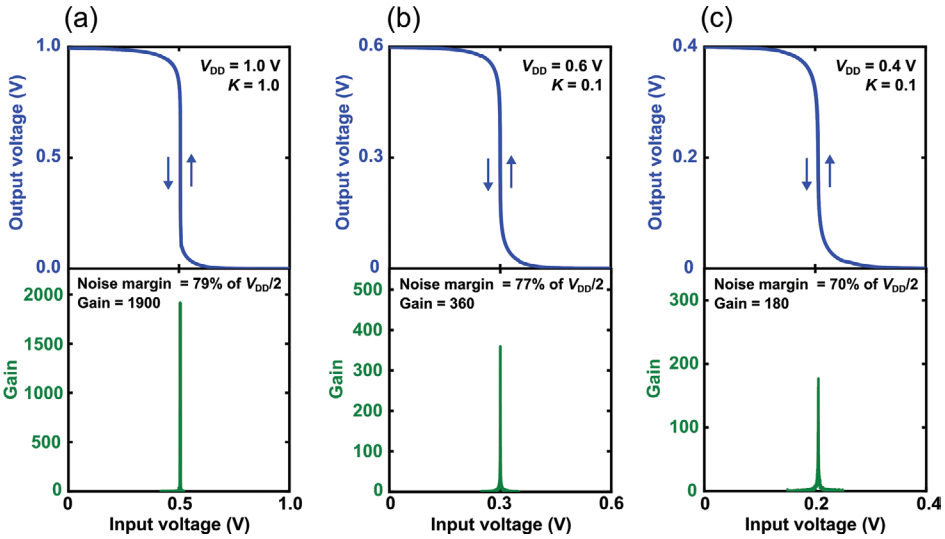

Figure 8. Measured transfer characteristics of zero-V_{GS} inverters based on DPh-DNTT TFTs with Ti/TiO_x/SAM and Al/AlO_x/SAM gate stacks for the load and drive TFTs, respectively.

normally-on load TFT (Ti gate electrode) and a normally-off drive TFT (Al gate electrode) on a flexible PEN substrate.

Figure 7b,c illustrates the dependence of the switching voltage of the zero-V_{GS} inverters on the channel-width ratio ($K = W_{load}/W_{drive}$) and the supply voltage (V_{DD}). For the optimum channel-width ratio K, the deviation of the switching voltage from its optimum value (i.e., from half the supply voltage, $V_{DD}/2$) ranges from 1 to 10 mV (or from 0.2% to 2.8%), depending on the supply voltage. All else being equal, a smaller deviation of the switching voltage from $V_{DD}/2$ will lead to larger noise margins. The optimized zero-V_{GS} inverters reported here have noise margins as large as 79% of $V_{DD}/2$ (determined using the method described in reference 33).

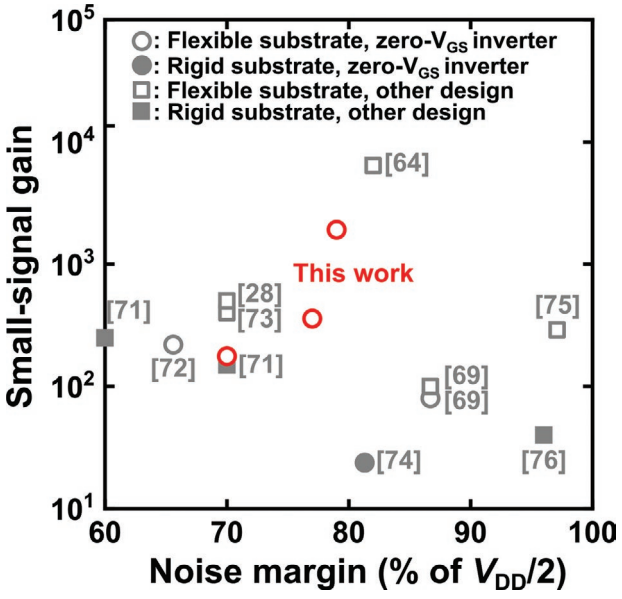

Figure 9. Literature summary of organic-TFT-based unipolar inverters with a small-signal gain of at least 10 and a noise margin of at least 60% of half the supply voltage.

Compared with diode-load and biased-load inverters, zero-V_{GS} inverters provide significantly larger small-signal gains.[69] The small-signal gains of the zero-V_{GS} inverters in **Figure 8** range from 180 at a supply voltage of 0.4 V to 1900 at a supply voltage of 1.0 V. **Figure 9** and Table S1 (Supporting Information) illustrate that the combination of low operating voltage, large noise margin and large small-signal gain of the inverters reported here compares very favorably with the performance of organic-TFT-based unipolar inverters reported in literature.

3. Conclusions

In summary, we have shown that it is possible to fabricate gate dielectrics with both high capacitance and low charge leakage by using plasma-grown titanium oxide in a hybrid TiO_x/SAM dielectric for use in flexible ultralow-voltage organic TFTs. We have presented flexible DPh-BTBT TFTs with a Ti/TiO_x/SAM gate stack and channel lengths as small as 0.7 µm that exhibit record organic-TFT-performance, including a channel-width-normalized transconductance of 0.6 S m^{-1} and an on/off current ratio of 10^7 for a gate-source-voltage range from 0 to –1 V, and a subthreshold swing at the room-temperature limit of 59 mV $decade^{-1}$.

In addition, we demonstrated unipolar inverters by combining DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack (normally-on load transistor) and an Al/AlO_x/SAM gate stack (normally-off drive transistor). These inverters combine large small-signal gains and large noise margins at ultra-low supply voltages of 1 V or less. The DPh-DNTT TFTs have channel-width normalized contact resistances as low as (12 ± 2) Ω cm, which is the smallest contact resistance reported to date for flexible organic TFTs in the linear regime of operation.

4. Experimental Section

Device Fabrication: All capacitors, TFTs and inverters were fabricated on flexible polyethylene naphthalate (PEN) with a thickness

of 125 µm (Inabata Europe GmbH, Düsseldorf, Germany). For the bottom electrodes of the capacitors and the gate electrodes of the TFTs, titanium with a thickness of 25 nm was deposited by thermal evaporation in vacuum (10^{-7} mbar) with a deposition rate of 1 to 2 nm s^{-1}. The TiO_x dielectric was produced by exposing the titanium surface to a capacitively coupled radio-frequency (13.56 MHz) plasma in pure oxygen (partial pressure 0.01 mbar) for a duration of 30, 60, 120, or 180 s at a plasma power of 200 W.[24] To produce a hybrid TiO_x/SAM dielectric, the substrate was then immersed into a 2-propanol solution of either *n*-tetradecylphosphonic acid or *n*-octadecylphosphonic acid (PCI Synthesis, Newburyport, MA, USA) to form a self-assembled monolayer. For the top electrode of the capacitors and the source and drain contacts of the TFTs, gold with a thickness of 30 nm was deposited by thermal evaporation in vacuum with a rate of 0.03 nm s^{-1}. To functionalize the source and drain contacts of the TFTs with a monolayer of pentafluorobenzenethiol (PFBT; TCI Deutschland GmbH, Eschborn, Germany), the substrate was immersed into a 0.01 M solution of PFBT in ethanol for 1 h.[21] As the semiconductor, a nominally 35-nm-thick layer of either 2,7-diphenyl[1]benzothieno[3,2-b][1]benzothiophene (DPh-BTBT; Sigma Aldrich) or 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f] thieno[3,2-b]thiophene (DPh-DNTT; Nippon Kayaku, kindly provided by K. Ikeda) was deposited by thermal sublimation in vacuum (10^{-7} mbar) with a deposition rate of 0.03 nm s^{-1}. During the semiconductor deposition, the substrate was held at a constant temperature of 100 °C for DPh-BTBT and 90°C for DPh-DNTT. Gate electrodes, source/drain contacts and organic-semiconductor layers were patterned using silicon stencil masks. These masks were fabricated from silicon-on-insulator (SOI) wafers by a combination of electron-beam lithography and deep reactive-ion etching of 20-µm-thick silicon membranes,[77,78] a process developed originally for ion-projection lithography.[79] Mask alignment was performed manually under an optical microscope.

Electrical Characterization: The capacitance measurements were performed using a Hameg HM8118 LCR meter, and the current-voltage measurements were performed using an Agilent 4156C Semiconductor Parameter Analyzer, both controlled using the software "SweepMe!" (https://sweep-me.net). All measurements were performed in ambient air at room temperature under yellow laboratory light.

Surface Characterization: The AFM images were recorded using a Bruker Dimension Icon Atomic Force Microscope in peak force tapping mode. Water contact-angle measurements were performed using a Krüss contact angle measurement system. A Zeiss Merlin Scanning electron microscope was used to perform the SEM investigations.

TEM Characterization: The TEM specimen was prepared by focused ion beam (FIB) in situ lift-out using a FEI Scios DualBeam instrument. The TEM image was recorded using a JEOL JEM ARM200F image-corrected atomic-resolution microscope and an acceleration voltage of 200 kV. Spatially resolved electron energy-loss spectroscopy for elemental mapping was conducted in scanning mode by raster-scanning the focused electron probe across the area of interest while acquiring energy-loss spectra for each spatial pixel.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

gate dielectric, low-voltage operation, organic transistor, subthreshold swing

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Supporting Information

Subthreshold Swing of 59 mV/decade in Nanoscale Flexible Ultralow-Voltage Organic Transistors

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Contents

1. Surface roughness

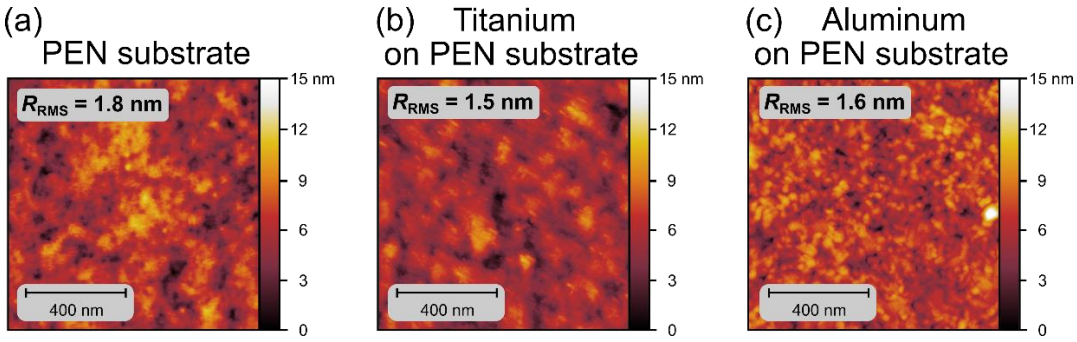

Figure S1. Atomic force microscopy (AFM) images and root-mean-square surface roughness of (a) the surface of a PEN substrate, (b) a 25-nm-thick vacuum-deposited titanium film on PEN, and (c) a 25-nm-thick vacuum-deposited aluminum film on PEN.

2. Error calculation for the permittivity of TiO_x

For calculating the permittivity of the oxide, the following theoretical relation between the unit-area oxide capacitance and the oxide thickness is fitted to the measurement data:

$$C_{\mathrm{ox}} = \varepsilon_0 \varepsilon_{\mathrm{ox}} \frac{1}{t_{\mathrm{ox}}}$$

As a consequence, the linear fit in the $C_{\mathrm{ox}}(1/t_{\mathrm{ox}})$-plot must go through the origin ($1/t_{\mathrm{ox}} = 0$, $C_{\mathrm{ox}} = 0$). This boundary condition significantly narrows the range of reasonable fit lines compared to what might have been expected from looking at the data points and their error bars with bare eyes. To illustrate this, we have plotted in the two graphs below the fit lines which correspond to $\varepsilon = 13$ and $\varepsilon = 15$ (i.e., $\varepsilon = 14 \pm 1$; Figure S2(a)) and to $\varepsilon = 12$ and $\varepsilon = 16$ (i.e., $\varepsilon = 14 \pm 2$; Figure S2(b)). By fitting the theoretical formula to the data (using the "Orthogonal Distance Regression" algorithm)[S1] and taking into account the error bars, we obtain an error of 0.6 for the permittivity. We have rounded this value up and report a permittivity of 14 ± 1 for the TiO_x.

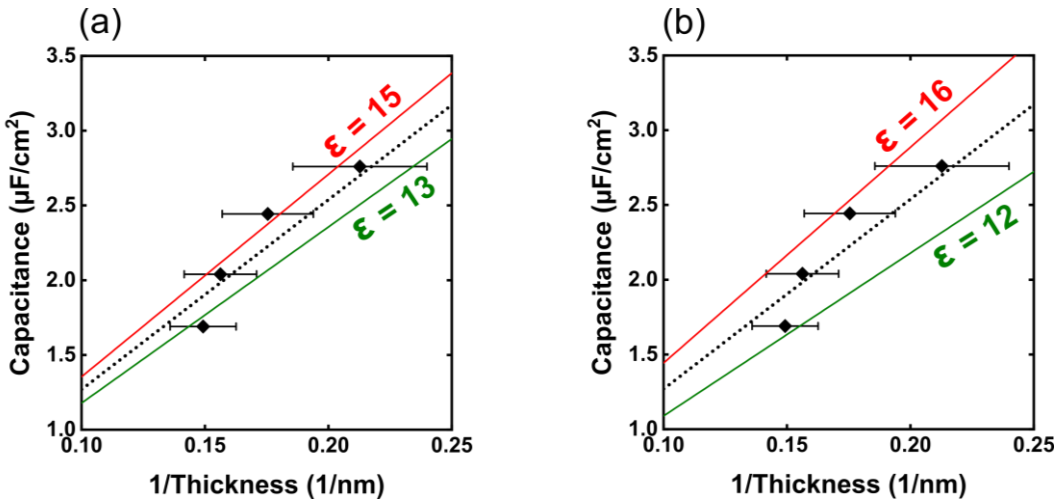

Figure S2. (a) Measured unit-area capacitance of capacitors based on bare plasma-grown TiO_x plotted as a function of the inverse of the TiO_x thickness, as determined by TEM, to calculate the relative permittivity of the plasma-grown titanium oxide. Shown is the fit which yields the total least squares of the orthogonal distance regression (black dashed line) and fit lines which correspond to $\varepsilon = 13$ and $\varepsilon = 15$ (i.e., $\varepsilon = 14 \pm 1$). (b) Fit lines which correspond to $\varepsilon = 12$ and $\varepsilon = 16$ (i.e., $\varepsilon = 14 \pm 2$).

3. Temporal evolution of the width-normalized contact resistance

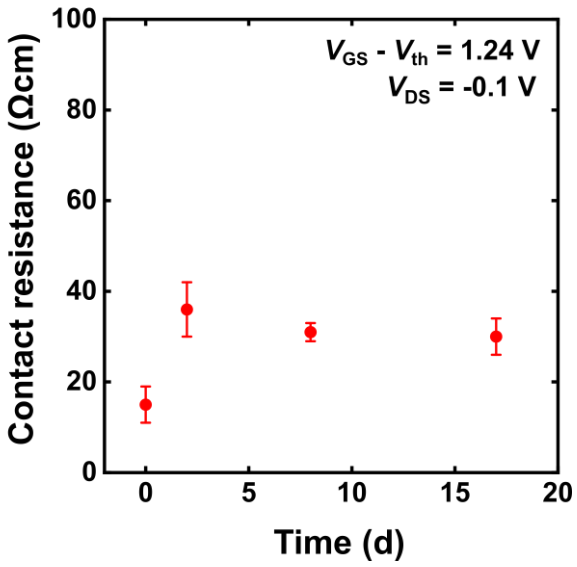

Figure S3. Evolution of the width-normalized contact resistance of flexible DPh-DNTT TFTs with a Ti/TiO_x/SAM gate stack over a period of 17 days after fabrication while being stored in ambient air with a relative humidity of about 40%.

4. Summary of unipolar inverters

Table S1. Summary of the parameters of the unipolar inverters from Figure 9.

Ref.	Substrate	Circuit design	# of TFTs	Supply voltage (V)	Small-signal gain	Noise margin (% of $V_{DD}/2$)
[28]	Flexible PEN	Pseudo-CMOS	2	2	500	70
[64]	Flexible PEN	Level-shift	4	20	6400	82
[69]	Flexible PI/BCB	Zero-V_{GS}	2	3	80	87
[69]	Flexible PI/BCB	Pseudo-D	2	3	100	87
[71]	Glass	Pseudo-CMOS	4	1	150	70
[71]	Glass	Pseudo-CMOS	4	1.5	250	60
[72]	Flexible PC	Zero-V_{GS}	2	4	220	66
[73]	Flexible PI	Pseudo-CMOS	4	2	400	70
[74]	Si wafer	Zero-V_{GS}	2	20	24	82
[75]	Flexible PI	Pseudo-CMOS	4	3	290	97
[76]	Si wafer	Pseudo-CMOS	4	20	40	96
This work	Flexible PEN	Zero-V_{GS}	2	1	1900	79
This work	Flexible PEN	Zero-V_{GS}	2	0.6	360	77
This work	Flexible PEN	Zero-V_{GS}	2	0.4	180	70

5. Implementation of the TFT-fabrication process in a manufacturing environment

The process for the fabrication of the organic TFTs described here is in principle similar to the process for the fabrication of organic light-emitting diodes in commercially manufactured active-matrix organic light-emitting diode (AMOLED) displays. All of the functional materials (gate electrodes, source/drain contacts, and organic semiconductor in the case of the organic TFTs; red, green and blue organic emitters in the case of AMOLED displays) are sequentially deposited by thermal evaporation or sublimation in a vacuum cluster system and patterned using stencil masks. This process avoids the use of resists, solvents and irradiation, all of which are potentially harmful to organic semiconductors, as well as the costs associated with the disposal of potentially toxic, carcinogenic and/or environmentally harmful chemicals often used in solution processing. The main difference between the TFT-fabrication process described here and the commercial OLED-fabrication process is that the display industry utilizes substrates with a size on the order of 1 square-meter and stencil masks made from invar metals[S2,S3] (fine-metal mask; FMM) that are aligned using automated vision systems and which provide a resolution on the order of 10 µm, whereas the TFT process described here is limited to a substrate size of a few square-centimeters and manual mask alignment, while providing a resolution of about 1 µm. Implementing this TFT process in a commercial manufacturing environment would thus make it possible to take advantage of rapid automatic mask alignment, but will likely lead to a compromise in terms of the TFT channel length (by using the larger-area commercial metal masks instead of the silicon masks employed here), unless the metal-mask resolution can be further improved. The plasma-oxidation process described here for the growth of the TFTs' gate oxide would require the addition of a plasma chamber to the cluster tool in which the depositions of the organic and inorganic materials are performed in commercial AMOLED display manufacturing. The formation of the thiol and phosphonic acid monolayers for the contact treatment and the gate dielectric, respectively, which in the work described here were carried out by immersing the substrates into ethanol or 2-propanol solutions, can alternatively be accomplished by a combination of vacuum deposition and thermal treatment,[S4] which are processes that can also be integrated into existing commercial cluster-tool process flows.

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