APPLIED SCIENCES AND ENGINEERING

# High-gain, low-voltage unipolar logic circuits based on nanoscale flexible organic thin-film transistors with small signal delays

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**One of the circuit topologies for the implementation of unipolar integrated circuits (circuits that use either p-channel or n-channel transistors, but not both) is the zero-$V_{GS}$ architecture. Zero-$V_{GS}$ circuits often provide excellent static performance (large small-signal gain and large noise margins), but they suffer from the large signal delay imposed by the load transistor. To address this limitation, we have used electron-beam lithography to fabricate zero-$V_{GS}$ circuits based on organic transistors with channel lengths as small as 120 nm on flexible polymeric substrates. For a supply voltage of 3 V, these circuits have characteristic signal-delay time constants of 14 ns for the low-to-high transition and 560 ns for the high-to-low transition of the circuit's output voltage. These signal delays represent the best dynamic performance reported to date for organic transistor–based zero-$V_{GS}$ circuits. The signal-delay time constant of 14 ns is also the smallest signal delay reported to date for flexible organic transistors.**

## INTRODUCTION

Thin-film transistors (TFTs) based on conjugated organic semiconductors can typically be fabricated at relatively low process temperatures, usually around or below 100°C and, thus, not only on glass but also on polymeric substrates (*1*). This makes organic TFTs potentially useful for flexible electronics applications, such as rollable active-matrix displays (*2*) and bendable integrated circuits (*3*, *4*). Choosing appropriate organic semiconductors makes it possible to fabricate both p-channel and n-channel organic TFTs (*5*), which, in principle, allows for the design and implementation of integrated circuits in a complementary circuit topology (*6*–*10*). Compared to unipolar circuits (which comprise only one type of transistor, either p-channel or n-channel) (*3*, *4*), complementary circuits have the advantage of providing inherently lower static power consumption (*11*).

However, the performance of even the best n-channel organic TFTs reported to date (*12*) is still notably inferior to that of state-of-the-art p-channel organic TFTs, with a performance gap of about one order of magnitude in terms of both charge-carrier mobility (about 10 $cm^2$/Vs for p-channel and 1 $cm^2$/Vs for n-channel organic TFTs) and contact resistance [10 ohm·cm for p-channel and above 100 ohm·cm for n-channel organic TFTs (*13*–*17*)]. As a result, the dynamic performance of organic complementary circuits is usually limited by the performance of the n-channel TFTs. For example, for unipolar ring oscillators (based on p-channel organic TFTs with a channel length of 1 μm) and complementary ring oscillators (based on p-channel and n-channel organic TFTs with the same channel length), signal propagation delays per stage of 580 ns (unipolar) and 6 μs (complementary) were recently reported (*18*). These results imply that there is an incentive for the development of unipolar circuits based solely on p-channel organic TFTs.

Unipolar circuits can be designed in a variety of circuit architectures, which differ mainly in the implementation of the load device (*19*–*21*). In terms of maximizing the small-signal gain and the noise margin (arguably the two most critical static-performance parameters of digital logic circuits), the zero-$V_{GS}$ design is generally considered a good choice. For example, we recently reported organic TFT–based zero-$V_{GS}$ inverters with a small-signal gain of 1900 and a noise margin of 79% of half the supply voltage (at a supply voltage of 1 V) (*15*). This is the best combination of these two parameters reported to date for organic TFT–based inverters (unipolar or complementary), with the exception of the positive-feedback level-shift design proposed by Raiteri *et al.* (*4*), which showed a small-signal gain of 6400 and a noise margin of 82% of half the supply voltage (for a supply voltage of 20 V). For comparison, the largest small-signal gain reported to date for organic complementary circuits is 1600 for circuits on glass (*22*) and 380 for circuits on flexible substrates (*23*), and the largest reported noise margin is 92.5% (*22*).

The principal drawback of the zero-$V_{GS}$ architecture is the large signal delay that occurs when the output node is discharged through the zero-$V_{GS}$ load transistor, while the drive transistor is nonconducting (*24*). The reason why the signal delay of the load transistor is typically larger in circuits based on the zero-$V_{GS}$ architecture than in circuits based on other architectures (all else being equal) is that the gate-source voltage of the load transistor is zero. In other circuit architectures, such as the biased-load architecture (*14*) and the saturation-load (or diode-load) architecture (*25*), the load transistor is usually biased with a larger gate-source voltage and thus can have a substantially larger transconductance and, hence, a smaller signal delay. Unfortunately, biased-load and saturation-load circuits suffer from inherently poor gain and small noise margin (*4*, *19*–*21*, *25*); in other words, they provide excellent dynamic performance but poor static performance.

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To take advantage of the superior static performance of zero-$V_{GS}$ circuits while markedly improving their dynamic performance, we have used electron-beam lithography to fabricate organic transistors with a very small channel length. To illustrate the benefits of reducing the channel length of the transistors, we provide here a comparison of organic inverters based on the zero-$V_{GS}$ architecture fabricated by shadow-mask lithography (using polyimide shadow masks with a resolution of about 20 μm) and electron-beam lithography (providing a resolution of about 100 nm). This reduction in channel length has led to a reduction in the signal delay of the inverters by approximately three orders of magnitude, resulting in a minimum signal-delay time constant of 14 ns at a supply voltage of 3 V.

## RESULTS

### Device fabrication

The key to fabricating zero-$V_{GS}$ circuits with optimum static and dynamic performance is to implement normally-off (enhancement-mode) drive transistors (to provide a switching voltage close to half the supply voltage and, thus, a large noise margin) and normally-on (depletion-mode) load transistors (to facilitate rapid discharging of the output node when the drive transistor is nonconducting).

For circuits based on p-channel (as opposed to n-channel) TFTs, this implies that the drive TFTs need to have a negative turn-on voltage and the load TFTs need to have a positive turn-on voltage. When logic gates based on the zero-$V_{GS}$ architecture are implemented using drive TFTs and load TFTs that have the same turn-on voltage, the small-signal gain can still be quite large (*26*), but the noise margin will usually be too small to allow cascading of logic gates into more complex circuits.

As reported previously (*15*), organic TFTs that have either a negative or a positive turn-on voltage can be fabricated by implementing two different gate stacks, for example, by fabricating the drive TFTs (which need to have a negative turn-on voltage) with an aluminum gate electrode in combination with a gate dielectric consisting of aluminum oxide ($AlO_x$) and a phosphonic acid self-assembled monolayer (SAM) and the load TFTs (which need to have a positive turn-on voltage) with a titanium gate electrode in combination with a $TiO_x$/SAM gate dielectric. This arrangement is schematically depicted in Fig. 1.

For the circuits investigated here, the TFTs were fabricated on flexible polyethylene naphthalate (PEN) substrates in the inverted coplanar (bottom-gate, bottom-contact) device architecture using the vacuum-deposited small-molecule semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT) (*27*). DPh-DNTT was chosen here for its relatively low contact resistance (*14*, *15*), although a similar performance (within a factor of approximately 2 to 5) can be expected using, e.g., DNTT (*18*, *19*). The gate metals (Al and Ti) were deposited by thermal evaporation in vacuum. The gate oxides ($AlO_x$ and $TiO_x$) were produced by exposing the surface of the gate electrodes to oxygen plasma (*28*) and functionalized with a SAM of an alkyl or a fluoroalkylphosphonic acid (*29*). The hybrid oxide/SAM gate dielectrics have a thickness of about 9 nm and a unit-area capacitance of 0.5 to 0.8 μF/cm$^2$, depending on the gate oxide and the phosphonic acid. In terms of surface roughness, surface energy, and insulating properties, the characteristics of the $AlO_x$/SAM and the $TiO_x$/SAM hybrid dielectrics are very similar (*15*). The surface of the gold source and drain contacts was functionalized with a chemisorbed monolayer of pentafluorobenzenethiol (PFBT), with the intention of minimizing the contact resistance of the TFTs (*30*).

### TFTs and circuits fabricated by shadow mask lithography

Figure 2 shows the measured transfer and output characteristics of DPh-DNTT TFTs fabricated by shadow-mask lithography. These TFTs have a channel length of 40 μm, a channel width of 200 μm, and gate-to-source and gate-to-drain overlaps of 15 μm. As can be seen, the TFTs with the Al/$AlO_x$/SAM gate stack have a negative turn-on voltage, and the TFTs with the Ti/$TiO_x$/SAM gate stack have a positive turn-on voltage, exactly as desired for the implementation of zero-$V_{GS}$ circuits with large noise margins (*15*). The difference between the turn-on voltages is about 0.8 V. The TFTs have charge-carrier mobilities and subthreshold swings of 4.5 cm$^2$/Vs and 75 mV/decade for the Al/$AlO_x$/SAM gate stack and 3.5 cm$^2$/Vs and 70 mV/decade for the Ti/$TiO_x$/SAM gate stack.

Figure 3 summarizes the electrical characteristics of a zero-$V_{GS}$ inverter and a two-input NAND gate fabricated by shadow-mask lithography. The drive TFTs, which need to have a negative turn-on voltage, were implemented using the Al/$AlO_x$/SAM gate stack,

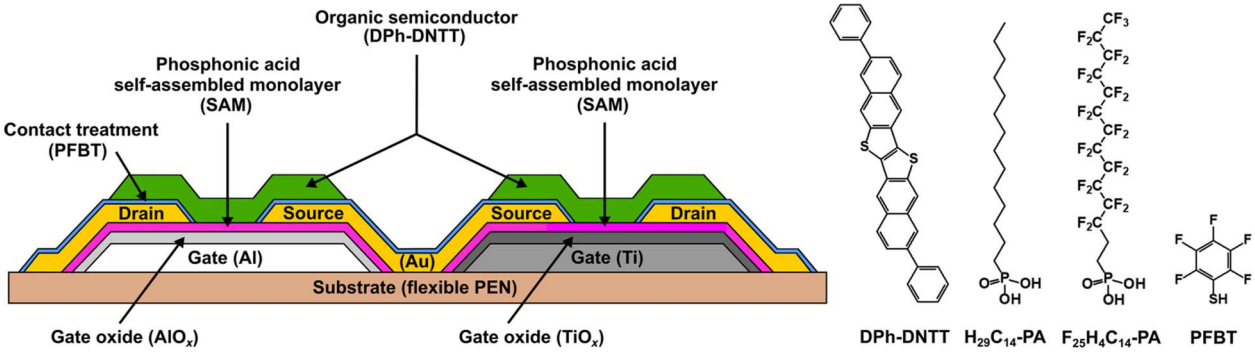


**Fig. 1. Device architecture and organic materials.** Schematic cross section of organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) device architecture with different gate stacks (Al/$AlO_x$/SAM and Ti/$TiO_x$/SAM) and thus different turn-on voltages, which makes this arrangement suitable for the implementation of zero-$V_{GS}$ circuits. Also shown are the chemical structures of the molecules used for the organic semiconductor (DPh-DNTT), the SAM of the gate dielectric (alkyl and fluoroalkylphosphonic acids), and the functionalization of the source and drain contacts with the intention of minimizing the contact resistance (PFBT).

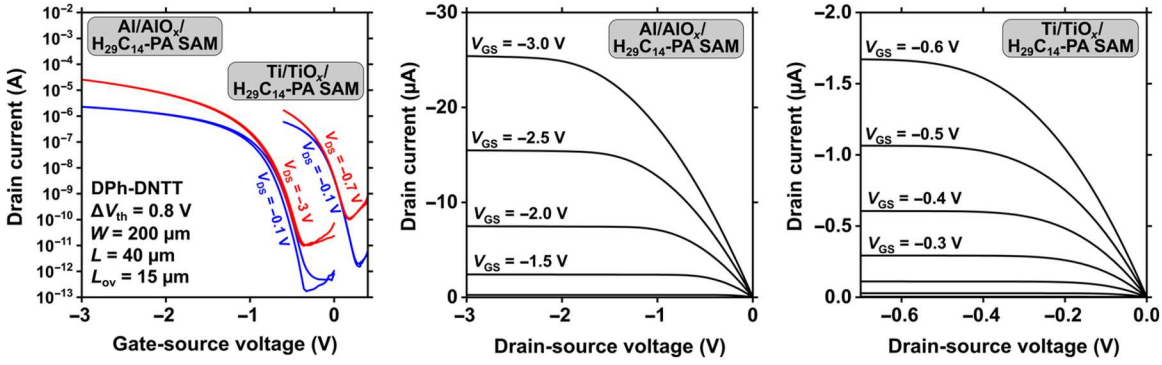


**Fig. 2. Static performance of TFTs fabricated by shadow mask lithography.** Measured transfer and output characteristics of DPh-DNTT TFTs with two different gate stacks fabricated by shadow-mask lithography. The TFTs have a channel length of 40 μm and gate-to-source and gate-to-drain overlaps of 15 μm. For this particular semiconductor (DPh-DNTT), the Al/$AlO_x$/SAM gate stack leads to a negative turn-on voltage and the Ti/$TiO_x$/SAM gate stack to a positive turn-on voltage, which makes this combination of TFTs suitable for the implementation of zero-$V_{GS}$ circuits. The difference between the turn-on voltages is about 0.8 V.

and the load TFTs, which need to have a positive turn-on voltage, with the Ti/$TiO_x$/SAM gate stack. The TFTs have a channel length of 20 μm, a channel width of 200 μm, and gate-to-contact overlaps of 15 or 20 μm. For a supply voltage of 1 V, the inverter provides a small-signal gain of 3200 and a noise margin of 80% of half the supply voltage. This is the best combination of small-signal gain and noise margin reported to date for organic TFT–based zero-$V_{GS}$ circuits (*15*).

To evaluate the dynamic performance of the inverters, a square-wave voltage with an amplitude of 1 V (equal to the supply voltage) was applied to the input node of the inverter, and the output response was measured using an oscilloscope. From the inverter′s output response, a characteristic signal-delay time constant (τ) of 70 μs was extracted for the low-to-high transition of the inverter′s output voltage (during which the output node is charged through the drive TFT) and 170 μs for the high-to-low transition (during which the output node is discharged through the load TFT while the drive TFT is nonconducting). As a result of these large signal delays, the operation frequency of these circuits is limited to approximately 500 Hz at a supply voltage of 1 V. In other words, the circuits have excellent static characteristics (large small-signal gain and large noise margin) but poor dynamic performance.

## TFTs and circuits fabricated by electron beam lithography

To obtain zero-$V_{GS}$ circuits with better dynamic performance, we used electron-beam lithography to pattern the gate electrodes and the source and drain contacts during the device fabrication process (*31*), which makes it possible to fabricate TFTs with channel lengths and gate-to-contact overlaps as small as about 100 nm. Figure 4 illustrates the capabilities of this process for fabricating dense arrays of TFTs and circuits with good accuracy on flexible polymeric substrates.

Figure 5 shows the measured transfer and output characteristics of DPh-DNTT TFTs fabricated by electron-beam lithography. These TFTs have a channel length of 2 μm, a channel width of 80 μm, and gate-to-source and gate-to-drain overlaps of about 100 nm. The TFTs have on/off current ratios between $10^6$ and $10^8$ and subthreshold swings of 85 mV/decade (Al/$AlO_x$/SAM gate stack) and 100 mV/decade (Ti/$TiO_x$/SAM gate stack). The difference in turn-on voltage obtained with the two different gate stacks is about 1 V. Results from an array of 10 TFTs with a channel length of 400 nm are summarized in Fig. 6.

Using the transmission line method (TLM) in the linear regime of operation performed on TFTs with channel lengths ranging from 80 nm to 2 μm, we determined channel width–normalized contact resistances of 1.1 kilohm·cm for the TFTs with the Al/$AlO_x$/SAM gate stack and 5.5 kilohm·cm for the TFTs with the Ti/$TiO_x$/SAM gate stack (see Fig. 7). These contact resistances are smaller than those in about 65% of all previous publications in which the contact resistance of organic TFTs has been reported, and they are within two orders of magnitude of the smallest contact resistances reported to date for organic TFTs (*14*, *15*, *30*). As discussed previously (*31*), the combination of electron-beam lithography and lift-off for the fabrication of organic TFTs possibly leads to relatively sharp contact edges (*32*) and possibly to residual contamination of the contact surfaces, which might explain why the contact resistance is not as small as what has been reported for organic TFTs fabricated by other methods (*14*, *15*, *30*). Because low contact resistances are the key to achieving useful dynamic performance (*33*), future work should thus focus on further reductions of the contact resistance.

Figure 8 shows the measured transfer characteristics of zero-$V_{GS}$ inverters based on DPh-DNTT TFTs with channel lengths of 1 μm and 130 nm. The TFTs have gate-to-source and gate-to-drain overlaps of about 80 nm and a channel width of 80 μm. The small-signal gain (80 for a channel length of 1 μm; 5 for a channel length of 130 nm) and the noise margin (74 and 28% of half the supply voltage, respectively) of these inverters are notably smaller than those of the inverters fabricated by shadow-mask lithography shown in Fig. 3. The small-signal gain of zero-$V_{GS}$ circuits is related to the subthreshold swing of the TFTs that are used in the circuits, and because the subthreshold swing of the nanoscale TFTs reported here (140 to 170 mV/decade) is notably larger than that of the long-channel TFTs shown in Fig. 2 (70 to 75 mV/decade), the small-signal gain of the nanoscale TFT–based inverters in Fig. 8 is smaller than that of the long-channel TFT–based inverters in Fig. 3. Nevertheless, the small-signal gain and the noise margin shown in Fig. 8 represent the best values reported to date for unipolar logic circuits based on organic TFTs with such small channel lengths.

To evaluate the dynamic performance of the zero-$V_{GS}$ inverters fabricated by electron-beam lithography, a square-wave voltage with an amplitude ranging from 1 to 4 V (equal to the supply voltage)

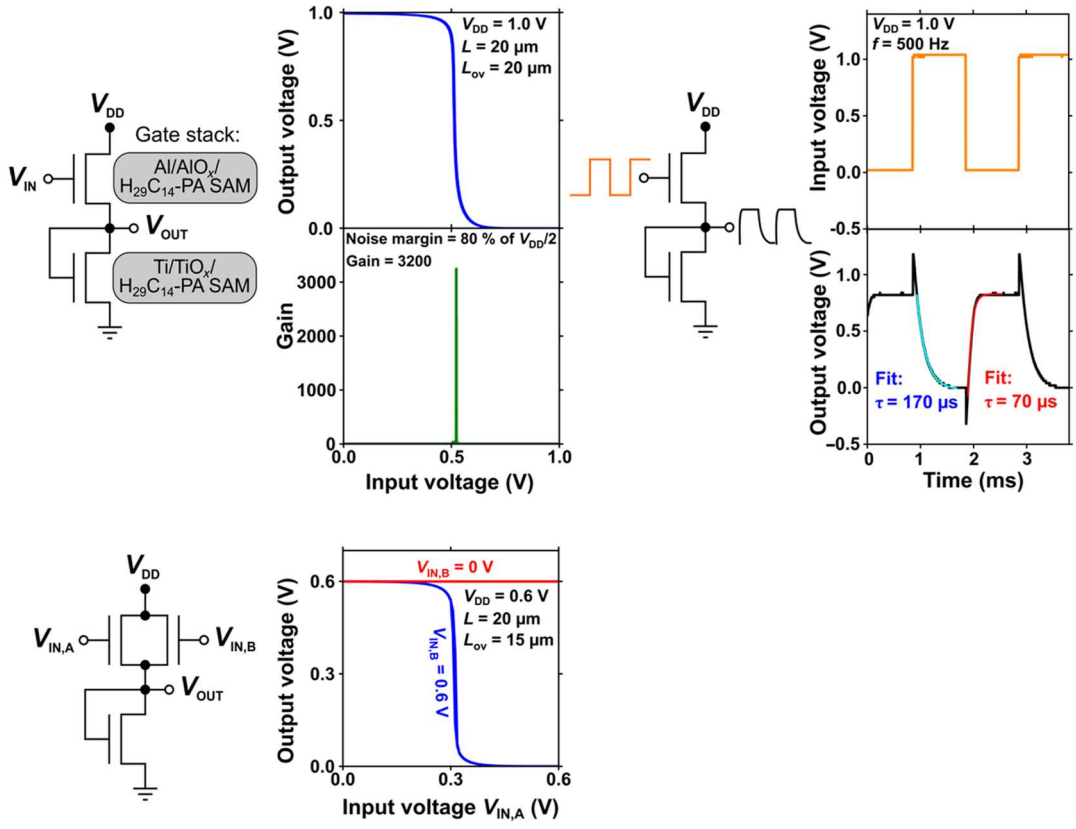


**Fig. 3. Static and dynamic performance of logic gates fabricated by shadow mask lithography.** Measured electrical characteristics of zero-$V_{GS}$ inverters and two-input NAND gates based on TFTs with a channel length of 20 µm. The combination of small-signal gain (3200) and noise margin (80% of half the supply voltage) represents the best static performance reported to date for organic TFT–based zero-$V_{GS}$ logic circuits. However, due to the large channel length of the TFTs, the dynamic performance of these circuits is quite poor (characteristic signal-delay time constants of 70 and 170 µs).

was applied to the input node of the inverter, and the output response was measured using a high-impedance probe and an oscilloscope. From the measured output response, the characteristic signal-delay time constants of the low-to-high transition (when the output node is charged through the drive TFT) and of the high-to-low transition (when the output node is discharged through the load TFT) were extracted. Results obtained from an inverter based on TFTs with a channel length of 120 nm and gate-to-contact overlaps of 90 nm are summarized in Fig. 9. For a supply voltage of 3 V, characteristic signal-delay time constants of 14 and 560 ns have been extracted for the low-to-high and the high-to-low transition, respectively. This is the best dynamic performance reported to date for zero-$V_{GS}$ circuits based on organic TFTs. The signal-delay time constant of 14 ns is also the smallest signal delay reported to date for flexible organic transistors and for lateral organic transistors. For vertical organic permeable-base transistors fabricated on glass, record signal delays of 8 and 5 ns have been reported for supply voltages of 3 and 4 V, respectively (*34*). A complete literature summary of organic TFTs for which signal delays below 50 ns have been reported is provided in Table 1. The signal-delay time constant (τ) of 14 ns reported here corresponds to an equivalent frequency [$f_{eq}$ = 1/(2·τ)] of 36 MHz at a supply voltage of 3 V, which corresponds to a voltage-normalized equivalent frequency of 12 MHz/V.

The characteristic signal-delay time constant of the low-to-high transition ($\tau_{rise}$) of the inverter's output voltage shows a strong

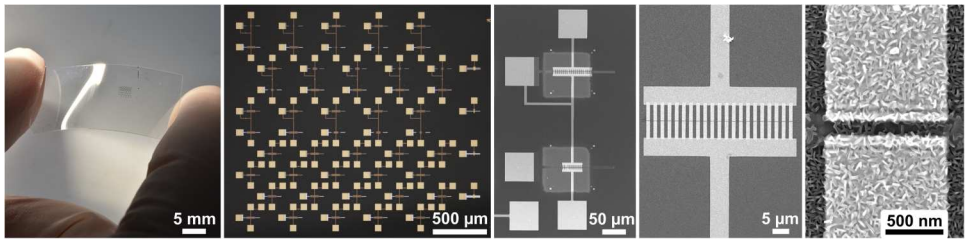


**Fig. 4. Devices and circuits fabricated by electron beam lithography.** Photographs and scanning electron microscopy images of organic TFTs and logic gates fabricated by electron-beam lithography on flexible, transparent PEN substrates.

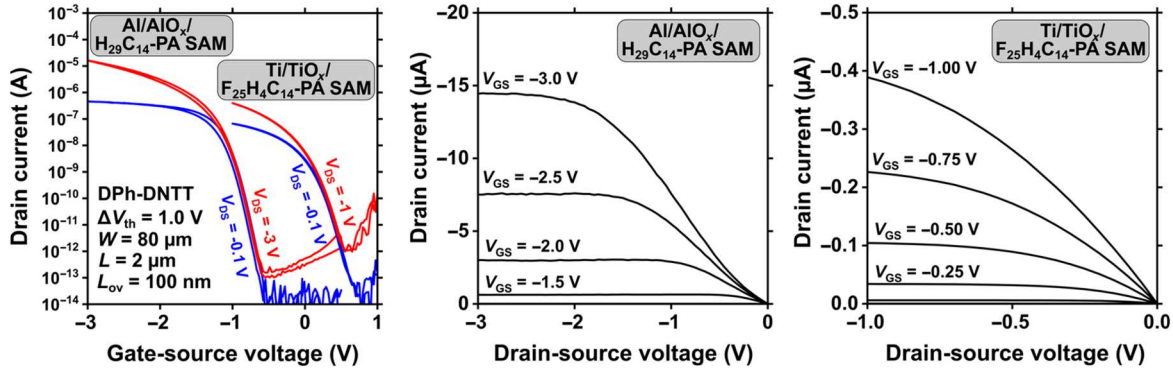


**Fig. 5. Static performance of TFTs fabricated by electron beam lithography.** Measured transfer and output characteristics of DPh-DNTT TFTs with two different gate stacks fabricated by electron-beam lithography. The TFTs have a channel length of 2 µm and gate-to-source and gate-to-drain overlaps of about 100 nm. The difference between the turn-on voltages is about 1 V.

dependence on the supply voltage ($V_{DD}$). This is the expected behavior because a larger supply voltage translates into a larger gate-source voltage on the drive TFT and, hence, a smaller signal delay when the inverter's output node is charged through the drive TFT. In contrast, the signal-delay time constant of the high-to-low transition ($\tau_{fall}$) shows very little variation with the supply voltage. This is due to the fact that the gate-source voltage on the load TFT, through which the inverter's output node is discharged when the drive TFT is nonconducting, is always equal to zero, i.e., independent of the supply voltage. A very weak dependence of the signal-delay time constant of the high-to-low transition ($\tau_{fall}$) on the supply voltage can be seen, which is due to the fact that the supply voltage affects the drain-source voltage on the load TFT, and this effect on the drain-source voltage of the load TFT leads to a weak effect on this TFT's signal delay.

## DISCUSSION

Whenever possible (i.e., when both p-channel and n-channel transistors with adequate performance are available), integrated circuits should be designed in a complementary topology, to take advantage of the inherently low static power consumption of complementary circuits. However, when a lack of either p-channel or n-channel transistors with sufficient performance or stability makes it necessary to consider unipolar circuit designs, the zero-$V_{GS}$ architecture is generally a good choice. As we have shown above, organic TFT–based zero-$V_{GS}$ circuits can provide excellent static performance, in terms of providing small-signal gains and noise margins that are at least on par with those of organic complementary circuits and substantially larger than what can be expected from biased-load or saturation-load circuits. The positive-feedback level-shift design proposed by Raiteri *et al.* (*4*) and the pseudo–complementary metal-oxide semiconductor architecture (*35*–*38*) are alternative unipolar-circuit concepts that have also demonstrated the ability to provide excellent static performance, albeit at the expense of a larger transistor count compared to the complementary and the zero-$V_{GS}$ architectures.

A weakness of the zero-$V_{GS}$ architecture is the large signal delay of the load TFT, which is a consequence of the fact that its gate-source voltage is always zero. Increasing the channel width of the load TFT will increase not only its transconductance but also its capacitance, so this will have little or no effect on the signal delay. One way to increase the transconductance of the zero-$V_{GS}$ load TFT without increasing its capacitance is to increase the absolute value of its turn-on voltage, and all else being equal, this should lead to a smaller signal delay. An attempt in this direction was made here by functionalizing the gate oxide of the load TFTs of the inverters shown in Figs. 8 and 9 with a fluoroalkyl SAM, rather than an alkyl SAM (*11*), but the effect of this was found to be rather limited.

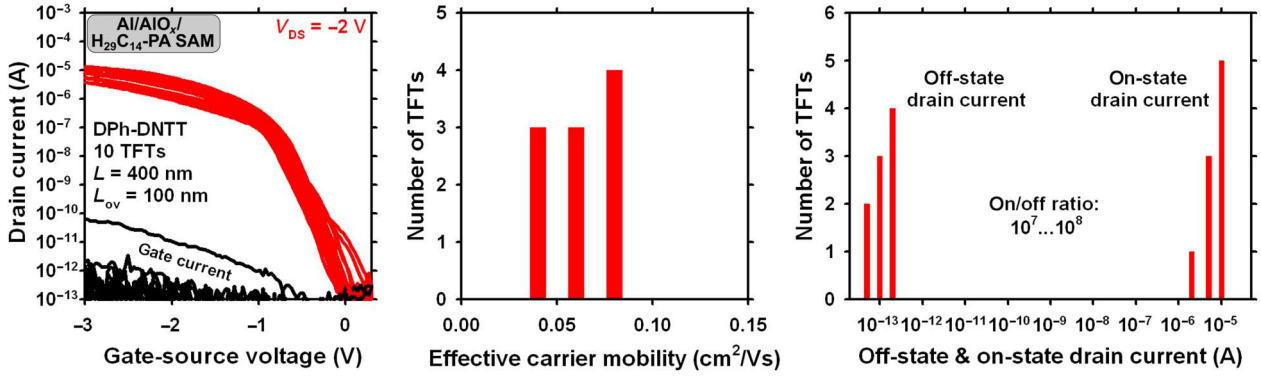


**Fig. 6. Parameter uniformity of TFTs fabricated by electron beam lithography.** Measured transfer characteristics of 10 nominally identical DPh-DNTT TFTs with an Al/AlO$_x$/SAM gate stack fabricated by electron-beam lithography. The TFTs have a channel length of 400 nm and gate-to-source and gate-to-drain overlaps of about 100 nm.

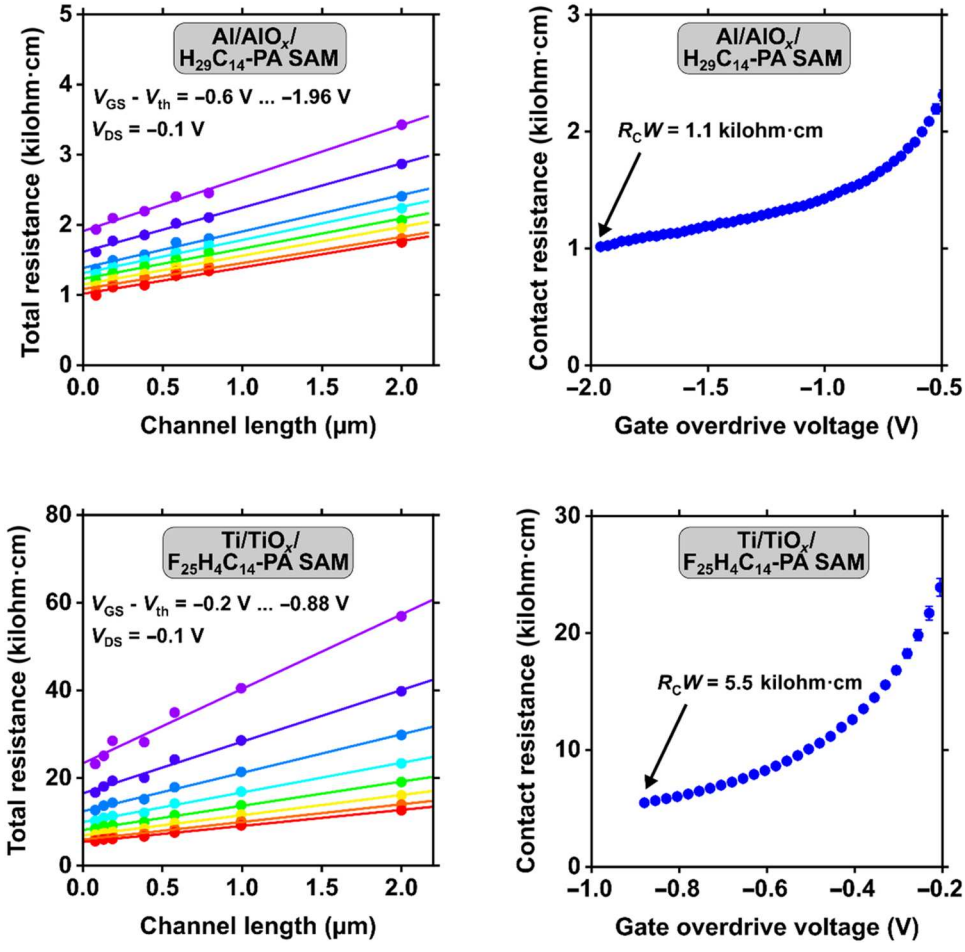


**Fig. 7. Contact resistance.** TLM analysis of DPh-DNTT TFTs fabricated by electron-beam lithography. Channel width–normalized contact resistances of 1.1 and 5.5 kilohm·cm are extracted for the TFTs with the Al/AlO$_x$/SAM gate stack and the Ti/TiO$_x$/SAM gate stack, respectively.

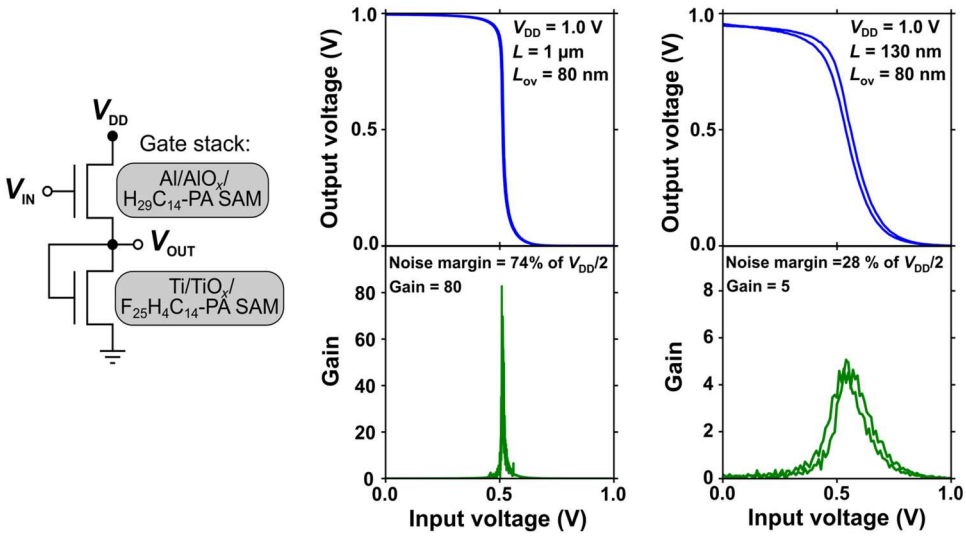


**Fig. 8. Static performance of inverters fabricated by electron beam lithography.** Measured transfer characteristics of zero-$V_{GS}$ inverters based on organic TFTs with channel lengths of 1 μm and 130 nm fabricated by electron-beam lithography.

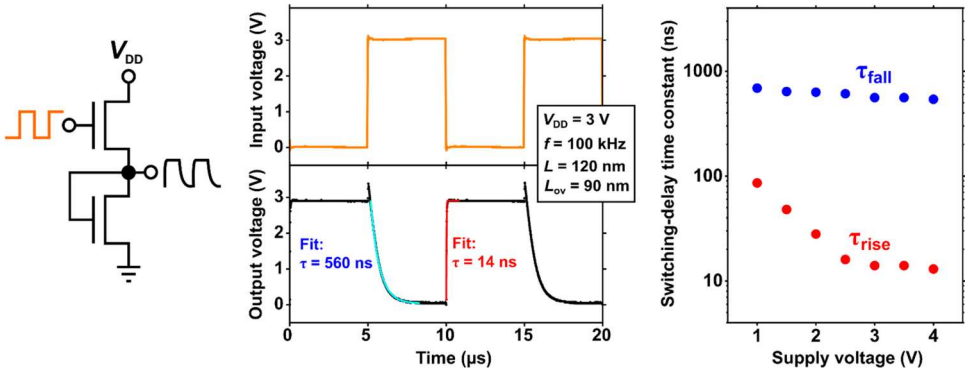


**Fig. 9. Dynamic performance of inverters fabricated by electron beam lithography.** Measured dynamic response of a flexible zero-$V_{GS}$ inverter based on DPh-DNTT TFTs with a channel length of 120 nm fabricated by electron-beam lithography.

**Table 1. Literature summary of signal delays below 50 ns measured in organic TFTs.** .

| Reference | Substrate | Transistor design | Inverter design | Patterning method | Channel length (μm) | Gate overlap (μm) | Contact resistance (ohm·cm) | Operation voltage (V) | Signal delay (ns) |
|---|---|---|---|---|---|---|---|---|---|
| (*34*) | Glass | Vertical | Complementary | Shadow masks | 0.5 | not applicable | not available | 4 | 5 |
| (*14*) | PEN | Lateral | Biased-load | Stencil lithography | 1 | | 10 | 2.5 | 19 |
| (*31*) | Glass | Lateral | Biased-load | E-beam lithography | 0.2 | 0.1 | 1000 | 2 | 40 |
| This work | PEN | Lateral | Zero-$V_{GS}$ | E-beam lithography | 0.12 | 0.09 | 1100 | 3 | 14 |

A more marked improvement in the dynamic circuit performance can be expected from reductions in the channel length of the TFTs. To explore this option, we have compared the performance of zero-$V_{GS}$ inverters based on organic TFTs with channel lengths of 20 μm (fabricated by shadow-mask lithography) and 120 nm (fabricated by electron-beam lithography). This reduction in channel length has led to a reduction of the signal-delay time constant of the high-to-low transition of the inverter's output voltage ($\tau_{fall}$) from 170 μs to 560 ns and of the signal-delay time constant of the low-to-high transition ($\tau_{rise}$) from 70 μs to 14 ns. This corresponds to an improvement by approximately three orders of magnitude.

This improvement in signal delay by approximately three orders of magnitude is due mainly to the reduction in the capacitance of the transistors. In the simplest circuit model, the signal delay is the product of the capacitance connected to the circuit's output node and the resistance through which this capacitance is charged or discharged during each switching event ($\tau = R{\cdot}C$). In zero-$V_{GS}$ inverters, the capacitance at the output node is approximately the sum of the capacitances of the two TFTs, minus their gate-source capacitances (*24*). For the work presented here, this output node capacitance is on the order of $10^{-10}$ F for the inverters fabricated by shadow-mask lithography and $10^{-13}$ F for the inverters fabricated by electron-beam lithography, i.e., smaller by about three orders of magnitude in the latter. When the input voltage of the inverter changes from high to low, this capacitance is charged through the drive TFT, which has an on-state resistance on the order of $10^5$ ohm (regardless of whether the TFTs were fabricated by shadow mask or electron-beam lithography in our experiments), so the signal delay for the low-to-high transition of the output voltage ($\tau_{rise}$) is on the order of $10^{-5}$ s for the inverters fabricated by shadow-mask lithography (measured: 70 μs) and $10^{-8}$ s for the inverters fabricated by electron-beam lithography (measured: 14 ns). When the input voltage of the inverter changes from low to high, the capacitance is discharged through the load TFT, which has an on-state resistance on the order of $10^6$ ohm, so the signal delay for the low-to-high transition of the output voltage ($\tau_{fall}$) is on the order of $10^{-4}$ s for the inverters fabricated by shadow-mask lithography (measured: 170 μs) and $10^{-7}$ s for the inverters fabricated by electron-beam lithography (measured: 560 ns). The measured values are thus reasonably close to the values predicted using the equation $\tau = R{\cdot}C$.

The fact that the on-state resistance of the TFTs reported here does not scale with the channel length is due to the fact that the drain current in the nanoscale TFTs is limited by the contact resistance, which is larger by about two orders of magnitude in the TFTs fabricated by electron-beam lithography than in the TFTs fabricated by shadow-mask lithography. If the contact resistance in the TFTs fabricated by electron-beam lithography was as small as that in the TFTs fabricated by shadow-mask lithography (i.e., on the order of 10 ohm·cm) (*14*, *15*), then the signal delays would be below 1 ns. This again illustrates the enormous incentive for further reductions in the contact resistance of nanoscale organic TFTs for gigahertz flexible circuits.

The nanoscale TFTs and inverters reported here were fabricated using electron-beam lithography. The main drawback of electron-beam lithography is its very low throughput. However, just like the throughput of other maskless patterning techniques, such as inkjet printing, can be greatly enhanced by the implementation of multiple nozzles, the efficiency of electron-beam lithography can be massively increased as well by implementing arrays of individually addressable electron beams. More than a dozen different multi-beam, multi-emitter, and multi-column designs have been developed (*39*), some of which are already commercially available. The throughput of these systems is, in principle, just as high as that of photolithography systems that use chrome-on-glass photomasks, and they provide almost the same resolution as the single-electron-beam lithography system used in the work reported here. Once these systems become more widely available, the commercial manufacturing of organic TFT–based integrated circuits using electron-beam lithography may, in fact, become practical.

## MATERIALS AND METHODS

All TFTs and circuits were fabricated on flexible PEN with a thickness of 125 μm (Inabata Europe GmbH, Düsseldorf, Germany). For the gate electrodes, aluminum or titanium with a thickness of 25 nm was deposited by thermal evaporation in vacuum ($10^{-7}$ mbar) with a deposition rate of 1 to 2 nm/s. The gate oxides ($AlO_x$ or $TiO_x$) were produced by exposing the surface of the gate electrodes to a capacitively coupled radio-frequency (13.56 MHz) plasma in pure oxygen (partial pressure 0.01 mbar) for a duration of 120 s at a plasma power of 200 W (*28*). To produce a hybrid oxide/SAM dielectric, the substrate was then immersed into a 2-propanol solution of either *n*-tetradecylphosphonic acid ($H_{29}C_{14}$-PA; PCI Synthesis, Newburyport, MA, USA) or 1*H*,1*H*,2*H*,2*H*-perfluorotetradecylphosphonic acid ($F_{25}H_4C_{14}$-PA; Specific Polymers, Castries, France) to form a SAM (*28*,*29*). For the source and drain contacts, gold with a thickness of 35 nm was deposited by thermal evaporation in vacuum with a rate of 0.03 nm/s. To functionalize the contacts with a monolayer of PFBT (TCI Deutschland GmbH, Eschborn, Germany), the substrate was immersed into a 10 mM solution of PFBT in ethanol for 1 hour (*14*). As the semiconductor, a nominally 40-nm-thick layer of DPh-DNTT [(*27*); Nippon Kayaku, provided by K. Ikeda, Y. Sadamitsu, and S. Inoue] was deposited by thermal sublimation in vacuum ($10^{-7}$ mbar) with a deposition rate of 0.03 nm/s. During the semiconductor deposition, the substrate was held at a temperature of 90°C. The gate electrodes and the source and drain contacts were patterned either using polyimide shadow masks (CADiLAC Laser, Hilpoltstein, Germany) (*10*) or by a combination of direct-write electron-beam lithography and lift-off (*31*). The current-voltage characteristics of the TFTs and the transfer characteristics of the inverters and NAND gates were recorded using an Agilent 4156C Semiconductor Parameter Analyzer. The noise margins of the inverters were calculated using the method described previously (*40*). The capacitance measurements were performed using a Hameg HM8118 LCR meter. Both the Agilent Semiconductor Parameter Analyzer and the Hameg LCR meter were controlled using the excellent software "SweepMe!" (https://sweep-me.net). The dynamic characteristics of the inverters were recorded using an Agilent 33250A Waveform Generator, a Textronix TDS 1001B Digital Oscilloscope, and a GGB Industries Model 19C Picoprobe. All electrical measurements were performed in ambient air at room temperature under yellow laboratory light using a manual probe station.

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