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Extraordinarily Weak Temperature Dependence of the Drain Current in Small-Molecule Schottky-Contact-Controlled Transistors through Active-Layer and Contact Interplay

Eva Bestelink, Hao-Jing Teng, Ute Zschieschang, Hagen Klauk, and Radu A. Sporea**

Low saturation voltages and extremely high intrinsic gain can be achieved in contact-controlled thin-film transistors (TFTs) with staggered device architecture, enabled by the energy barrier introduced at the source contact. The resulting device, the source-gated transistor (SGT), is limited in its usefulness by the high temperature dependence of the drain current induced by the source energy barrier. Here, the interaction between the thermal characteristics of the source contact and the semiconductor to show drastically reduced temperature dependence for SGTs based on organic semiconductors (OSGTs) is exploited. This extraordinarily weak temperature dependence of the drain current is observed regardless of the height of the source energy barrier (27.8% in OSGTs with Ti contacts compared to 22.1% when using Au contacts, over a 34 K range). The reduction in mobility of the semiconductor offsets an increase in thermionic-field emission of charge carriers at the source. This is a first for SGTs and provides a route to removing one of the last hurdles to their wider adoption. The OSGTs with Ti contacts also demonstrate: drain-current saturation at very low drain-source voltages (saturation factor of 0.22); noteworthy stability after 70 days; and minimal drain-current variation with channel length or illumination.

1. Introduction

Development of large-area electronics (LAE) based on organic semiconductors (OSC) has rapidly accelerated in recent years.[1] Valuable applications in lighting,[2] biosensing,[3] or security[4–6] arise from the versatile processability[7] of these materials, particularly when high-throughput methods, such as roll-to-roll or inkjet printing, are concerned.[8] Even in display technology, where uniformity is paramount, manufacturers have developed the capability of fully inkjet printing organic light emitting diodes (OLEDs)[9] toward producing cost-effective commercial displays. Yet, for future Internet of Things (IoT) applications, including biomedical or agricultural sensors, significant further development of such low-cost methods is essential. In particular, thin-film transistors (TFTs) require special focus, as the central building block of logic, decision, and signal processing functions.

Although seemingly facile, producing circuits comprising organic TFTs (OTFTs) via high-throughput methods remains challenging, particularly where device-to-device uniformity of operation and stability is concerned.[10] Still, in conventional vacuum processes, where breakthroughs in terms of reducing the contact resistance and increasing the charge–carrier mobility are promoting high-performance OTFTs,[11] the issues associated with uniformity and stability have persisted. In order to promote manufacturing yield of circuits, one approach would be to reduce the number of transistors used within the design.[12] Doing so, however, limits the designer's ability to create high-performance functions, for example by sacrificing the benefits from traditional cascode or multi-stage gain-enhancing techniques for signal conditioning. Thus, alternative solutions would be required.

Following recent developments in *n*-type OSCs, researchers have produced organic bipolar junction transistors (OBJTs).[13] While OBJTs may lead to faster switching speeds for wireless data, energy transmission, and may deliver high gain, the increase in processing steps would likely inflate manufacturing costs beyond limits of economic viability. Conversely, applications in biosensing rarely necessitate high cut-off frequency f_T, as signals are often in the low Hz to kHz range.[14,15]

Alternative high-gain TFT architectures have been developed, which can readily be fabricated alongside OTFTs in the same process. With only minor process adjustments, entirely different device operation can be obtained. Source-gated TFTs (SGTs)[16–21] and, indeed, organic SGTs (OSGTs, **Figure 1**a)[22–26] have recently captured the attention of researchers for their exceptionally low saturation voltages with extremely flat output

E. Bestelink, H.-J. Teng, R. A. Sporea
Advanced Technology Institute
University of Surrey
Guildford GU2 7XH, United Kingdom
E-mail: r.a.sporea@surrey.ac.uk
U. Zschieschang, H. Klauk
Max Planck Institute for Solid State Research
70569 Stuttgart, Germany
E-mail: h.klauk@fkf.mpg.de
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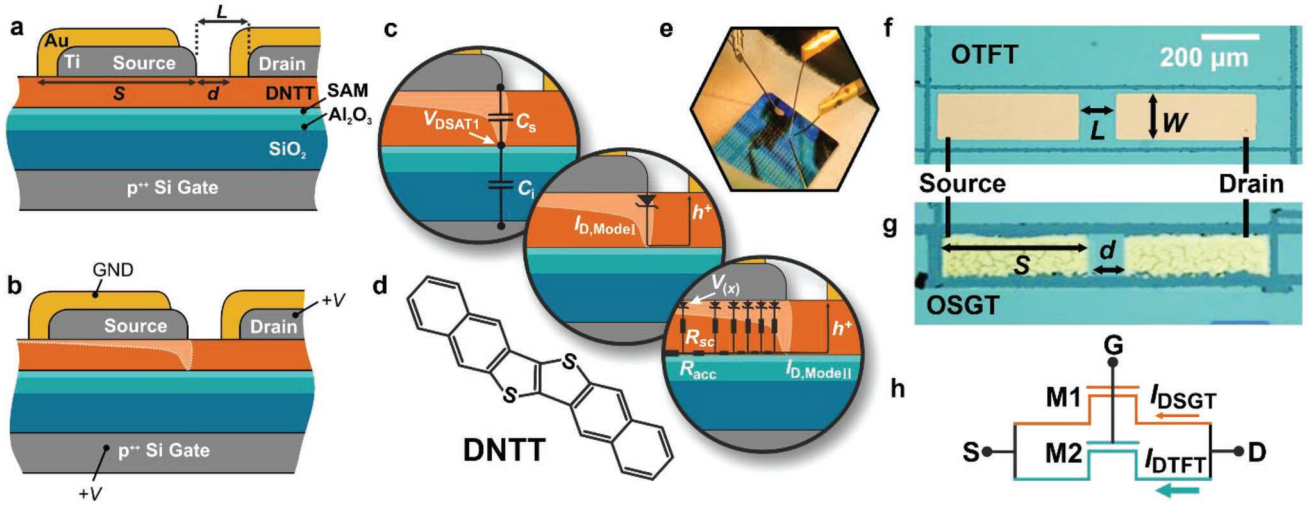

Figure 1. Cross-section schematics of organic source-gated transistors (OSGTs) showing a) constituent layers and design parameters, namely source-gate overlap *S*, source-drain separation *d*, and nominal channel length *L* (in absence of Au cap), and b) depletion envelope under the source edge when the Schottky source is reverse-biased by the drain potential during operation. For the devices considered here, the source-drain separation *d* of the OSGTs is smaller than the nominal channel length *L* of the organic thin-film transistors (OTFTs). c) Top left: pinch-off occurs under the source edge, and the saturation voltage V_{DSAT1} is determined by the series specific capacitances of the depleted semiconductor C_s and the gate insulator C_i. Middle: *Mode I* drain current is highly temperature-dependent due to thermionic-field emission of charge carriers over the barrier. Bottom right: *Mode II* injection is determined by the vertical and lateral resistance of the semiconductor R_{sc} and the accumulation layer R_{acc}, respectively. A portion of V_{DSAT1} is dropped along the bulk of the active layer $V_{(x)}$, facilitating injection. Furthest regions of *S* are less able to contribute to the process due to an extremely high resistance. d) Molecular structure of the organic semiconductor DNTT. e) Photograph of a substrate with organic transistors. f) Photograph of an OTFT with Au contacts. g) Photograph of an OSGT with Ti contacts and Au capping, showing *d* effectively shorter than *L*. OSGTs have been scored at the very edges of the contacts to prevent unwanted influence of Au in the barrier control and injection processes. h) Circuit schematic with OTFT as M1 and OSGT as M2 showing deleterious parallel conduction mechanism of the parasitic OTFT, obtained by direct contact of the Au with the active layer in the case of offset electrode evaporation, and eliminated by the edge scoring depicted in (g).

characteristics. However, among several key design criteria,[27] the superior analog performance of SGTs is primarily enabled by the deliberate introduction of a sizeable energy barrier at the source contact,[16,17,28] which is capable of fully depleting the semiconductor at the source edge (Figure 1b,c). Of several avenues into creating energy barriers at the source,[29–31] the simplest method would be to implement a Schottky contact. However, like many other contact-controlled devices with Schottky-contacts, the drain current displays a high temperature dependence,[18,32,33] due to increased thermionic-field emission, which is typically an undesirable effect, requiring additional circuit design techniques for compensation.

Here, we witness a breakthrough in the temperature dependence of contact-controlled devices, as a result of the interplay between a small organic molecule, dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT, Figure 1d,e),[34] and the interface of the Schottky-contact in an OSGT architecture, which leads to a substantially lower drain-current temperature dependence than expected from Schottky-contact SGTs. While source barriers with tunnelling layers have been proposed to eliminate temperature effects[29,30] by allowing charge carriers to tunnel at the position of the Fermi level,[29] here for the first time we have observed greatly diminished effects of the temperature on the saturated drain current in Schottky-contact OSGTs with a comparatively high source contact barrier.

In addition to overcoming a major hurdle for Schottky barrier devices, the fabricated transistors demonstrate additional SGT features in DNTT, which affirms their reputation for robust operation. Notably, resilience to threshold-voltage (V_{th}) shifts and improved stability in ambient air and with visible light illumination. As SGT operation differs substantially from conventional TFTs, which brings about these effects, we start by discussing the nature of its operating principles and highlight several design considerations, as demonstrated by electrical characterization of DNTT OSGTs and comparing results with those of DNTT OTFTs.

2. Source-Gated Transistors versus Thin-Film Transistors: Operation and Stability

OTFTs and OSGTs were fabricated on a heavily doped silicon substrate, which also serves as the gate electrode. The gate dielectric is a stack of thermally grown SiO_2 (100 nm thick), atomic-layer-deposited Al_2O_3 (8 nm thick), and an *n*-tetradecylphosphonic acid self-assembled monolayer (SAM, Figure 1a,e). The organic semiconductor DNTT was deposited by thermal sublimation in vacuum (25 nm thick). The Au or Ti source and drain contacts were deposited by thermal evaporation through a shadow mask. OTFTs and OSGTs were identical, except for the metal, where Au was used for OTFTs (Figure 1f), and Ti and Au were deposited sequentially (denoted TiAu) for OSGTs (Figure 1g). OSGTs were isolated by scoring at the contact edges to ensure the parasitic OTFT created by the Au capping metal and connected electrically in parallel with the OSGT did not overwhelm the OSGT drain current, (Figure 1h, see Experimental Section for full details). The transfer characteristic of the OTFT (**Figure 2**a) highlights the acceptable

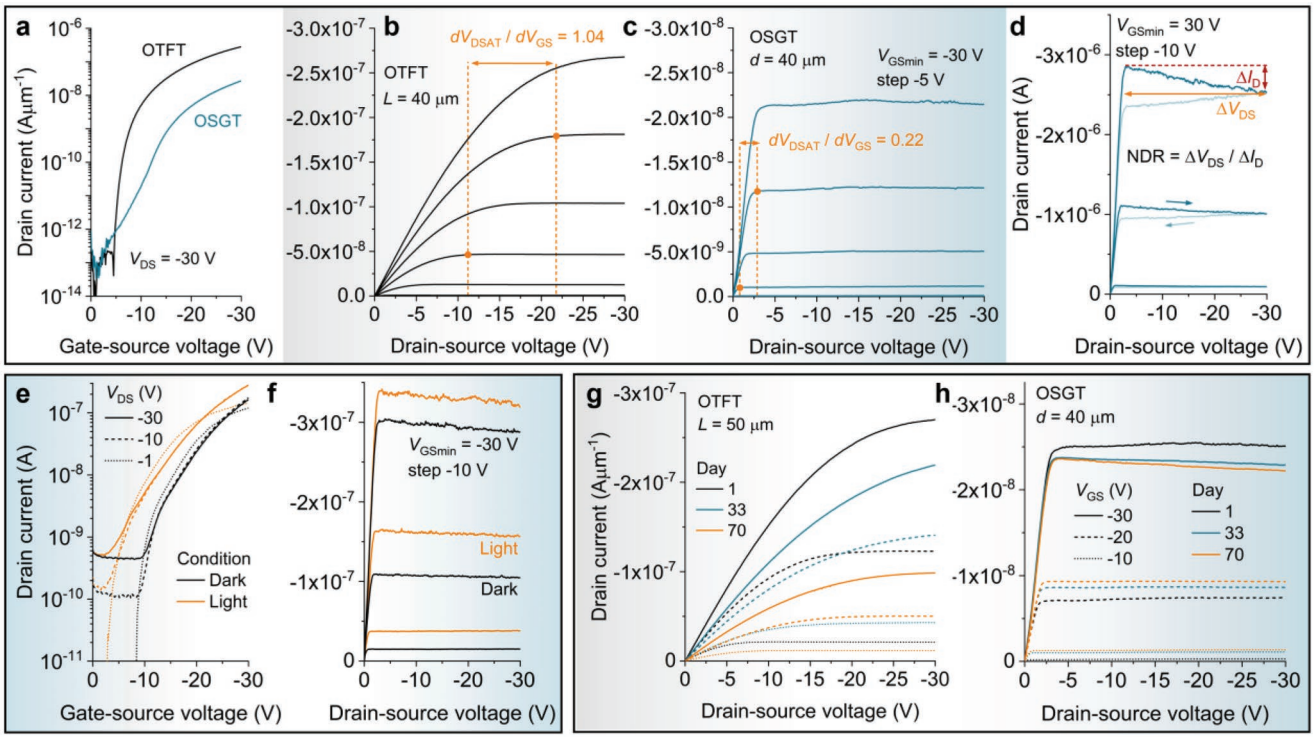

Figure 2. a) Comparison of the measured transfer characteristics of an OTFT and OSGT, showing the trade-off of the maximum drain current and the transconductance for other operational benefits, in the case of the OSGT. b) Measured output characteristics of the OTFT. c) Measured output characteristics of the OSGT, showing the smaller saturation voltage and larger intrinsic gain that typically accompany contact-controlled operation. d) Negative differential resistance (NDR) can be observed in some OSGTs. e) Transfer and f) output characteristics of OSGTs during operation in light and dark conditions, showing that NDR does not change under illumination. The drain-current levels do not differ significantly. Output characteristics for the g) OTFT and h) OSGT demonstrating robustness of the OSGT to storage in ambient.

subthreshold slope, given the low-capacitance gate-dielectric stack, as well as the suitable on/off ratio achievable through favourable contact and channel properties. In comparison, the OSGT transfer characteristic yields an increased subthreshold slope and reduced on-state drain current, both the result of an entirely different operating mechanism.

The differences between the two transistors are even more apparent in their output characteristics. Unlike TFTs, where drain-current saturation occurs when the channel is pinched off at the drain (Figure 2b), SGTs saturate when pinch-off occurs at the source (Figure 2c).[16] During operation, for a given gate-source voltage V_{GS}, the electric field produced by biasing the drain leads to a reverse-biasing of the rectifying source contact. Should the semiconductor be capable of being fully depleted across its entire thickness, the device will pinch-off at the edge of the source closest to the drain (Figure 1b).[28] Hence, the OTFT output characteristics (Figure 2b) saturate at the gate-overdrive voltage ($V_{DSAT2} = V_{OV} = V_{GS}–V_{th}$), while the OSGT (Figure 2c) saturates at the product of the gate-overdrive voltage and the series specific capacitances of the gate insulator (C_i) and the depleted semiconductor (C_s)[35] (Figure 1c, top left):

$$V_{DSAT1} = V_{OV}\left(\frac{C_i}{C_i + C_s}\right) + K \quad (1)$$

K is a constant that represents a small drain-source voltage V_{DS} for depleting additional charges that accumulate at the semiconductor-insulator interface.[35] By design, SGTs trade-off transconductance g_m to attain low-voltage saturation, as both properties are governed by the semiconductor-layer characteristics (thickness t_s, permittivity ε_i) and that of the gate-insulator stack (thickness t_i, permittivity ε_i).[36] The series specific capacitances effectively represent a saturation coefficient, $\gamma = (C_i/(C_i + C_s))$,[27] which can be calculated based on the layer properties. An effective means of evaluating saturation would be to estimate the V_{DSAT1} points from the set of output characteristics and calculate $\partial V_{DSAT} / \partial V_{GS}$.[17,27] In principle, for field-effect transistors (FETs) it is unity (Figure 2b), and for SGTs it should be γ. For the combination of layer properties considered here, the measured $\partial V_{DSAT} / \partial V_{GS}$ of 1.04 for the OTFT is close to the expected value of unity. For the SGT, the calculated γ is 0.26 (see Experimental Section for layer properties and Ref. [27] for further elaboration), which is in good agreement with the estimated $\partial V_{DSAT} / \partial V_{GS}$, for which a value of 0.22 is extracted (Figure 2c). This low-voltage saturation is obtained even as the OSGT drain current is only one order of magnitude smaller than that of the OTFT, conforming to our empirical experience that that extremely low V_{DSAT1} can only be obtained if the drain current is at least 10–30 times smaller than that of the Ohmic-contact OTFT with identical geometry (a schematic illustration of this behavior is given in Ref. [27]).

At drain-source voltages higher than the pinch-off voltage, there are two charge-injection mechanisms that occur simultaneously;[37] however, one will dominate over the other,

depending on the designed source-gate overlap, S.[28] Mode I injection (Figure 1c, middle) involves charge–carrier injection by means of thermionic-field emission over the energy barrier from the very edge of the source to within a few tens to a few hundreds of nanometers of S (depending on the active-layer thickness). As the injection is based on the Schottky effect, the drain current produced by this mode is highly temperature-dependent.[32] Mode II injection (Figure 1c, right), on the other hand, occurs within the bulk of the S overlap region and is governed not by the reverse-biased barrier, but rather by the vertical resistance (R_{sc}) of the partially-depleted semiconductor and the horizontal resistance in the accumulation layer at the semiconductor-insulator interface (R_{acc}).[37,38] This distributed network of resistances ($R_{(x)} = R_{sc(x)} + R_{acc\,(x)}$), together with a proportion of V_{DSAT1} ($V_{(x)}$), determines the drain current ($I_{D,Mode\ II}$) along the length of the source[28] (Figure 1c, right):

$$I_{D,ModeII} = \int_0^S \frac{V_{(x)}}{R_{(x)}} dx \tag{2}$$

Hence, S is a design parameter in SGTs, and $I_{D,Mode\ II}$ (and g_m, up to a point) will increase with S.[28,39] For very large S, however, there is insufficient vertical potential drop across the semiconductor layer to promote injection in the furthest regions.[28] Thus, $I_{D,Mode\ II}$ saturates at a value S_{SAT} and depends on the properties of the semiconductor, particularly the charge–carrier mobility. Considering that the minimum feature size when the source/drain contacts are patterned using contact photolithography is 1 to 2 µm, the vast majority of SGTs reported operate in Mode II, with an expectedly lower temperature dependence than Mode I.[32] When patterning the contacts using shadow masks, as is the case here, S is much greater (>50 µm), thus the devices would operate at S_{SAT}.

While SGTs are renowned for their ability to achieve record-high intrinsic gain (reaching ≈10^5 in SGTs based on polycrystalline silicon),[40] some of the OSGT output characteristics demonstrate an appreciable negative differential resistance (NDR), which increases with V_{OV} (Figure 2d). In TFTs, NDR typically occurs due to trap states at the semiconductor-insulator interface in the channel region;[41,42] however, the OTFT results here do not display any NDR. Seeing that SGTs are contact-controlled devices, the presence of trap states at the semiconductor-insulator interface is unlikely to be the case. Conversely, previous observations of high NDR with decreasing channel length[41] have been attributed to traps at the contact-semiconductor interface, which become more prominent as contact effects begin to emerge in conventional TFTs, which is the more likely scenario in the OSGTs. The use of back-scan traces (Figure 2d) and changing the lighting conditions[42] (Figure 2e,f) confirm the presence of traps at the interface between the Ti contact metal and the semiconductor DNTT, rather than at the semiconductor-dielectric interface, and these traps are responsible for the NDR observed in the output characteristics. Visible cracks on the electrodes (Figure 1g) are likely due to mechanical strain induced by the Ti deposition and subsequent inadvertent delamination of the semiconductor. These cracks would only result in a reduction in drain current due to discontinuities in the electric field,[32] which should not be V_{DS}-dependent. With process optimization, such devices would be capable of delivering the anticipated exceptionally flat characteristics of SGTs.

Finally, when comparing the electrical performance degradation over time, OTFTs (Figure 2g) suffer far worse, as the channel region is exposed directly to the ambient. The OSGT (Figure 2h) is considerably more resilient, as the injection region is largely screened by the source contact. As the semiconductor region between source and drain acts only as a parasitic series resistance in the on-state of the SGT,[43] it is reasonable to expect superior stability during storage. In fact, the OSGTs presented here only show a reduction in drain current with time for the lowest V_{GS} (11% decrease at $V_{GS} = -30$ V, $V_{DS} = -20$ V over a 70 day interval). At higher values of V_{GS}, the drain current demonstrates an increase of 25.5% ($V_{GS} = V_{DS} = -20$ V), whereas the drain current of the OTFT only decreases by 59.3%, worsening to 58.2% at the lowest V_{GS}. Although further investigation would be required to understand the superior OSGT stability, optimization in the processing of the contact metals may offer additional improvements, considering that, as is, the cracked surface observed in Figure 1g is likely exposing the active layer to ambient.

2.1. Device Geometry and its Effect on Drain Current

As discussed, in SGTs the source-gate overlap S is a design parameter, and the drain current increases with S up to a value of S_{SAT} at that there is no further contribution to the source region.[22,28,39] This feature is what gives rise to the ability of the SGT to provide the ultimate device-to-device uniformity of operation.[22] The device characteristics in **Figure 3** highlight this behavior.

As expected from the nature of its well-known operation, the OTFT drain current is dependent on the channel length L, and the threshold voltage V_{th} is prone to variations with L (Figure 3a,b). The OSGTs (Figure 3c,d) present minimal variations with geometrical source-drain gap d (distinct from the effective channel length L, which in SGTs may be pinched off at one or both ends). The output characteristics for both OTFTs (Figure 3b) and OSGTs (Figure 3d) for a single value of V_{GS} reveal that V_{DSAT} does not change appreciably with d (Figure 3e). The OTFT does follow the expected trend, with an L-dependent drain current (coefficient of determination (R^2) = 0.928 confirming a strong correlation), where discrepancies are likely due to V_{th} shifts in this case. The OSGT, without any emerging trend (Figure 3f), also follows its expected behavior (R^2 = 0.001 showing a negligible correlation), and discrepancies could either be due to minor V_{th} variations or barrier inhomogeneities, as a result of cracks in the contact metal. While d is not a design parameter in SGTs, it should be kept to a minimum to ensure the channel resistance is lower than that of the source contact.[38] In Figure 3d, the resistance created by large d results in a higher potential drop in the channel. Since higher V_{DS} are then needed to fully pinch-off the source, V_{DSAT} thus increases.

Since the source is the means by which injection is controlled in SGTs, Figure 3g presents results from devices made with other contact metals, where, in an ideal situation, the work function WF of the metal is the principal determinant of the effective energy barrier height at the metal/DNTT interface. However, this is not as straightforward in some cases, as interfacial states and chemistry will dictate the nature of the barrier.[44]

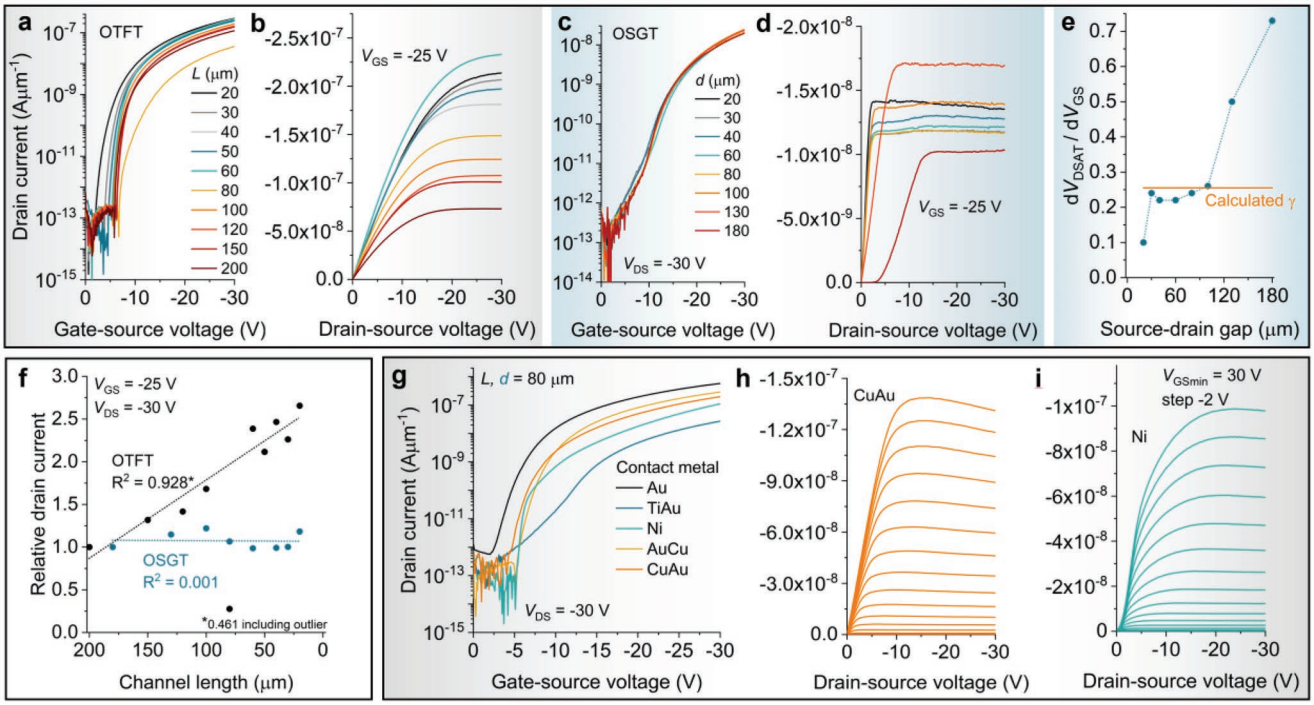

Figure 3. a) Transfer and b) output characteristics of OTFTs demonstrating the predicable behavior. c) Transfer and d) output characteristics of OSGTs. In SGTs, drain current does not vary with the source-drain gap d; however, for larger values of d, the increased resistance of the channel necessitate additional drain-source voltage V_{DS} to facilitate pinch-off. This explains the increase in V_{DSAT1} observed here. e) Plot of ∂V_{DSAT} / ∂V_{GS} showing that the saturation voltage is unaffected by d for small separations. The results are in good agreement when compared to the saturation coefficient γ. f) When compared to the drain current produced by the longest channel length L (or d in SGTs), the OTFT follows a 1 / L dependence, while the OSGT dependence is very weak and likely resulting from varying channel resistance. g) The effect of varying contact metal. In theory, the work function would determine the barrier height, but in reality, results can vary. h) Output characteristics of OTFTs with CuAu source/drain contacts show SGT-like curves. i) Ni contacts also produce contact-controlled behavior, where two saturation points can be observed.

In general, TFTs will operate via the field effect, with some degree of contact effects, which become more pronounced with increased barrier height. However, when the energy barrier is sufficiently large to allow full depletion of the active layer, it can lead to source pinch-off and contact-controlled operation. As such, V_{DSAT1} manifests itself at the expense of a decrease in on-state drain current, and there is generally a trade-off of a reduced current density, smaller g_m and smaller f_T for lower V_{DSAT1}. Interestingly, the output characteristics of OTFTs with CuAu contacts more closely resemble those of SGTs (Figure 3h), with a ∂V_{DSAT} / ∂V_{GS} ≈0.4. This observation fits with work function (WF) theory, as the work function of Cu is ≈4.65 eV,[45,46] which is sufficiently low to form a substantial barrier, but not as low as the work function of Ti (4.33 eV). In some cases (e.g., Ni contacts, WF ≈5.15 eV), two saturation points can be observed, namely V_{DSAT1} where the source pinches-off, followed by V_{DSAT2} when the channel pinches-off at the drain end (Figure 3i). The use of field-plate structures on the source[27,47] would help in this case to screen the injection area from the influence of the lateral electric field from the drain, facilitating flat saturation beyond V_{DSAT1}.

Evidence suggests that the large source-drain gap of these devices also prevents low-voltage saturation. OTFTs with Ni contacts and with CuAu contacts both have a significantly higher drain current density than the OSGT with the TiAu contacts. As a result, a larger potential drop in the channel region leaves insufficient drain voltage to fully pinch-off the source at the V_{DS} value predicted by the calculated γ.[38,48] In some cases, simply implementing a Schottky contact with a high barrier and/or reducing t_s to promote full source-side depletion is not sufficient to guarantee SGT operation.[27]

Once again, we see evidence of NDR in the output characteristics in Figure 3h,i. As both CuAu and Ni devices did not present with any cracks in the electrodes, the NDR here would be solely due to trap states at the DNTT/contact interface.

3. Temperature Behavior of DNTT OSGTs

The temperature dependence of the drain current of the DNTT OTFTs (**Figure 4**a,b) follows the previously reported behavior, where the drain current decreases with increasing temperature.[49] While literature generally favors the hopping model to explain a decrease in charge-carrier mobility with decreasing temperature, investigations of DNNT have shown bandlike transport,[50,51] which also supports these findings. Whichever the case, TFTs, and OTFTs by extension, are generally more temperature-stable than Schottky barrier-controlled transistors, which inherently possess a highly positive temperature dependence of their saturated drain current. In DNTT OTFTs, stable temperature behavior is achievable[49] and can be improved by reducing the DNTT-deposition rate,[52] which

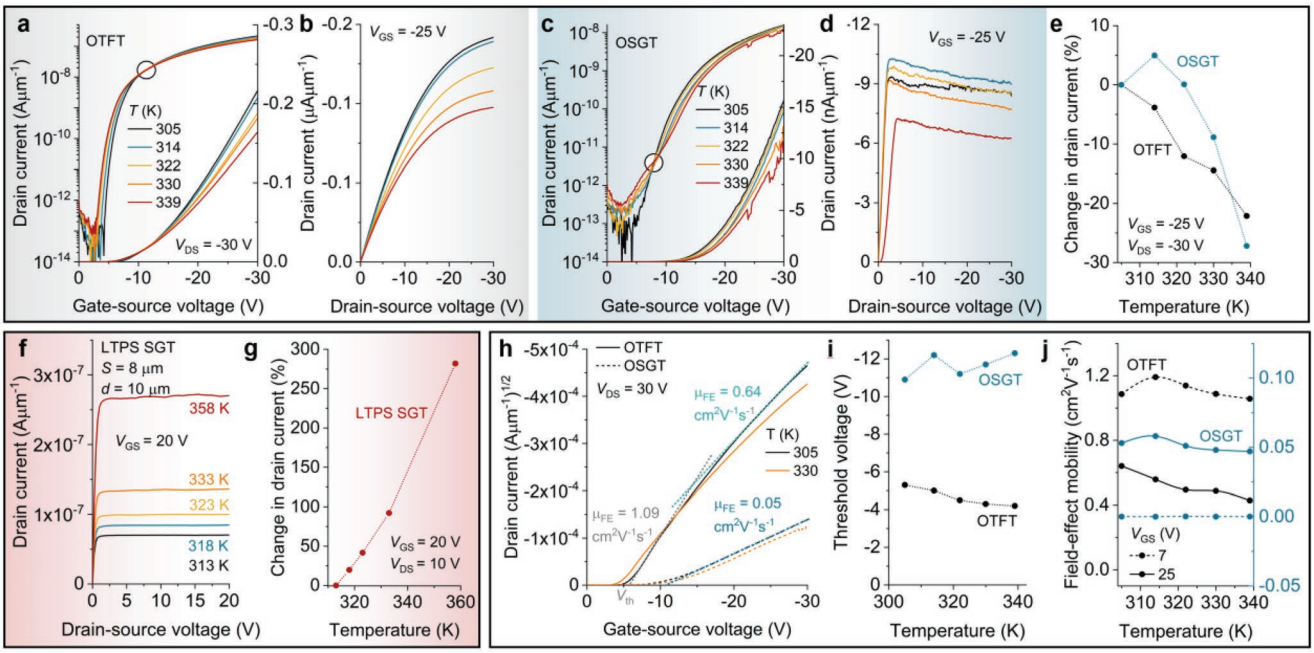

Figure 4. a) Transfer and b) output characteristics of the OTFT for various temperatures. The drain current follows that of previously reported devices and decreases with increasing temperature. c) Transfer and d) output characteristics of OSGTs, also demonstrating a reduction in drain current with increasing temperature. e) The drain current increases by only 5% for the first few Kelvin before decreasing. There is a large interval where the drain current is relatively stable compared to that of the OTFT. f) Output characteristics of a low-temperature polycrystalline silicon (LTPS) SGT with Schottky contacts, showing the predictable nature of its drain current. g) The LTPS SGT drain current increases by 20% in the first few Kelvin and reaches ≈280% change when compared to its baseline value. The DNTT OSGTs only change by 27%. h) Extracting field-effect mobility μ_{FE} is not straightforward, as mobility varies considerably in the OTFT depending on V_{GS}. i) V_{th} decreases with temperature in the OTFT, yet there is a general increase of a similar magnitude in the OSGT. j) Apparent field-effect mobility decreases in both the OTFT and OSGT at high V_{GS}, dominated by effects present in the active layer.

facilitates a higher degree of molecular order, as well as a lower contact resistance. In contrast, contact-controlled transistors rely on energy barriers at the source contact, and a reduction of these energy barriers is detrimental to their operation. While the high temperature dependence of SGTs can be exploited for temperature sensing[15] or highly compact circuits for regulating temperature,[15,53] in general, technologists might be reluctant to implement these devices, as circuits require stable operation of individual devices they comprise. Current-mode driving is one design solution to this problem. Indeed, matched low-temperature polycrystalline silicon (LTPS) Schottky barrier SGT current mirrors have demonstrated exceptional temperature-independent current copying.[15] However, most voltage-controlled applications would require fairly complex compensation techniques.

Here, the change in drain current with temperature shown by the DNTT OSGTs in Figure 4c,d is extraordinarily low for Schottky-contact devices (Figure 4e). While SGTs with long S overlaps do have a lower positive temperature coefficient, the devices here display a behavior unprecedented in Schottky-contact TFT design, with a temperature dependence closer to that of the OTFT, rather than a typical Schottky SGT. In Figure 4e, for an increase in temperature by 34 K, the drain current only changes by roughly 27%, of which it only increases by 5% in the first few Kelvin (305 to 314 K). For comparison, LTPS SGTs with Schottky contacts (see Experimental Section for details) show a significantly higher increase in drain current with temperature (Figure 4f), with the example here demonstrating an increase by 280% over a temperature interval of 44 K when compared to a reference temperature (Figure 4g), and the relative increase in drain current is roughly 20% for an initial 5 K interval from a 313 K reference. At higher temperatures, the drain current of the LTPS devices continues to increase supralinearly with temperature, as expected, yet in the DNTT OSGTs, the drain current instead decreases.

This highly unusual behavior may be a first for SGTs. Previous reports of temperature-related phenomena could aid in the understanding of the nature of this peculiarity. In Peng et al.,[54] Ohmic-contact DNTT OTFTs developed energy barriers at the source contact during temperature-dependent characterization, producing a sizeable reduction in field-effect mobility, as the contact effects were significant enough to produce output characteristics resembling those of SGTs, with two clear saturation points at V_{DSAT1} and V_{DSAT2}. When measuring the devices following a resting period, they reverted to regular Ohmic-contact behavior, indicating the induced energy barrier was not permanent. This "dynamic contact resistance"[54] may be part of the DNTT OSGTs' temperature behavior. As the temperature increases (Figure 4c–e), we see the first initial rise in drain current, even though it is much lower than expected. This may be due to the energy barrier at the source contact in the DNTT OSGTs, which increases simultaneously and thus restricts injection. Following this argument, at a temperature of ≈313 K, the barrier increase is higher than the temperature-

related injection that accompanies the Schottky-barrier lowering, and the drain current begins to decrease with increasing temperature. While it could be argued that an increased density of trap states at the semiconductor-insulator interface under temperature conditions might be responsible for the observed degradation in carrier mobility, the NDR in the output characteristics (Figure 4d) does not differ significantly to indicate additional trap states. It is more likely that the mobility of the OSC is changing due to other phenomena.

In a recent publication, Takimiya et al.[51] mention that an estimation of the electronic structure of DNTT is not straightforward, as the molecules are not static in their crystalline state but are rather "dynamically vibrating".[51] In their study, the authors fabricated DNTT OTFTs and confirmed the temperature-dependent mobility in DNTT and its derivatives, where changes in mobility occur as a result of electronic structure.

This is further evident in the topmost trace of the OSGT output family of curves with temperature shown in Figure 4d (red), where V_{DSAT1} increases. This is due to the parasitic channel resistance in the source-drain gap d, where the decrease in mobility of the DNTT leads to a larger proportion of potential being dropped across the channel, due to the decrease in conductivity of the material. As such, to fully-deplete the active layer at the source edge, higher V_{DS} is required, corresponding to the increase in V_{DSAT1}.

Hence, further insight can be gained from evaluating the effective field-effect mobility and threshold voltage; however, this is not straightforward. Typically, TFT field-effect mobility μ_{FE} and V_{th} are characterized through the FET gradual channel approximation and taking the square root of the transfer characteristic in the saturation regime, respectively. This has become standard practice across several technologies, including thin-film silicon, amorphous oxide semiconductors and 2D materials. However, contact effects are generally present to some degree in TFTs, and mobility is often overestimated,[55] especially in OTFTs, where source energy barriers are particularly salient. In SGTs, where operation is governed by the contact resistance, these approaches do not provide an accurate route to parameter extraction. While the apparent value of μ_{FE} extracted with the usual method does indeed correlate with the transconductance and the magnitude of the drain current (Figure 4h), it does not represent a physical description of the drift and diffusion processes within the channel. It does, however, allow comparison between transistors with different structures in terms of their net behavior. Similarly, the knee in the transfer characteristic of SGTs does not have the same physical meaning as the threshold of a TFT, representing the crossover point between the channel conductance and source region conductance as the limiting factor for total current through the transistor. In this work, we have chosen to use conventional methods for μ_{FE}/V_{th} comparison, acknowledging the limitations of the metrics.

In Figure 4h, the general approximation for assessing μ_{FE} and V_{th} in TFTs only applies for low values of V_{GS}. As μ_{FE} changes with V_{GS}, a single best fit line to obtain the gradient is not suitable. Hence, here we have included a second approximation at higher V_{GS}. While the μ_{FE} of the OTFT is not as high as previously reported (1.09 vs 2.96 $cm^2\ V^{-1}\ s^{-1}$) and V_{th} is more negative (−5.3 vs −1.37 V), these values are substantially greater than those of the OSGT (0.05 $cm^2\ V^{-1}\ s^{-1}$, Figure 4h, and −10.9 V, Figure 4i, respectively). Yet, the μ_{FE} reported for the OSGT is taken at higher V_{GS}, where the mobility for the OTFT drops significantly to μ_{FE} = 0.64 $cm^2\ V^{-1}\ s^{-1}$. The estimations at low V_{GS} in the OSGT are not directly comparable, as the device is operating in the subthreshold regime. As mentioned above, obviously μ_{FE} in the OSGT would be lower than that of the OTFT given the significantly lower g_m, but unlike the OTFT, OSGT μ_{FE} improves for higher V_{GS} (Figure 4j). This is due to the nature of SGT operation in disordered semiconductors, where high internal electric fields and lower charge injection lead to improved performance.[56] Moreover, μ_{FE} does not change as drastically as that of the OTFT with temperature, attesting to its reputation with respect to stability of operation. Regarding the temperature behavior of the OSGT, the change in μ_{FE} supports the behaviour seen in the output characteristics as per Figure 4d and corresponds to an increasing resistance in the OSC, which leads to the decrease in drain current and increased V_{DSAT1}. Together with the increased injection from the Schottky source contact, the interaction of these two processes presents an interesting, and notably practical, way of obtaining temperature characteristics of SGTs that are not dissimilar to those of the equivalent TFT. Although all Mode II drain current yields weaker temperature dependence, the comparisons from LTPS SGTs operating with Mode II cannot match the extremely favorable performance seen here, which would contribute to a design simplification while maintaining the benefits of low-voltage saturation and low output conductance.

A peripheral observation is highlighted by the circled regions of the transfer curves in Figure 4a and c. Both OTFT and OSGT manifest an operating point at that the drain current does not vary with temperature, consistent with observations of commercial silicon n-type metal-oxide-semiconductor field-effect transistors.[57] This point appears relatively close to the threshold voltage of the OTFT, but deep into the subthreshold region of the OSGT characteristics, confining its application to highly specialised ultralow-power circuits.[58,59]

4. Conclusion

In this study, we observe contact-controlled transistors with uncharacteristically low drain-current variation with temperature, through competing contact and semiconductor mobility effects.

DNTT TFTs fabricated in the staggered (bottom-gate, top-contact) device architecture with TiAu contacts show definitive contact-controlled behaviour, notably: low saturation voltage; drain-source voltage dependence in saturation; channel-length independence of drain current; stability under incident visible light; as well as excellent stability during storage in ambient air for over two months, with unusual behaviour that certainly warrants further investigation.

Critically, these OSGTs demonstrate a very weak variation of the drain current with temperature, despite a high Schottky energy barrier at the source. This behavior is comparable to that of Ohmic-contact TFTs with Au electrodes and arises from the interplay between the contact injection and lateral transport processes. While temperature-stable versions of DNTT TFTs

have been demonstrated,[51,52] the ability to exploit the change in effective carrier mobility to offset unwanted drain-current changes in OSGTs as a result of temperature variations is pivotal in the development of these devices. The co-optimisation of channel and source lengths should allow the complete balancing of these two effects in the relevant region of the transistor's operation. As the critical processes occur in the source region, the findings presented here are relevant to other contact-controlled architectures.[60] The ensuing high-gain, low-series-voltage, high-stability OSGTs will be instrumental in creating extremely versatile organic semiconductor-based circuits and systems.

The benefits enumerated above need to be put in balance with the practical limitations of the current fabrication approach.

To begin, the patterning of metals from two different sources via shadow masks is inherently problematic for scale-up and manufacturability, as sizeable offsets between the patterns are likely. In the x direction, the problem may be mitigated by the inherent tolerance of the SGT to source-drain gap variations.[22] Two cases are considered. First, one electrode will have Au extending into the channel, while bare Ti will exist on the other. If used as a source, the electrode with Au extension would not produce SGT behaviour due to (quasi-)Ohmic injection at the edge. This limits the use of that electrode as the drain, in which case the source will have a portion of exposed Ti. In turn, if the Ti extension oxidizes only partly at the surface over time, no change to operation would be observed. Should the whole exposed Ti area become non-conductive, the net effect would be an increase of the effective source-drain separation, up to the region of the same electrode that is covered by Au. In principle, the SGT design should tolerate this quite well, owing to contact-controlled current magnitude. Second, in the y direction, the difficulty of the offset metals is illustrated in Figure 1h. Even a narrow strip of Au in contact with the active layer would produce sufficient injection to overwhelm the control properties of the Ti electrode. There is no easy solution for this problem, but other techniques may be used to create the electrodes. In addition, it would be of interest to further explore the behavior with temperature of devices comprising other contact metals, for which the intermediate operation[37] between TFT and SGT regimes is encountered. Here, we have only focused on the likely extremes of this spectrum, however use of a single metal layer would avoid issues with unwanted offsets.

Next, we should consider restrictions imposed by the layer deposition and patterning during fabrication. Contact-controlled transistors, such as SGTs, require a staggered electrode configuration, which may limit the availability of techniques and materials/solvents that reliably work together within a process flow. Here, for convenience, we chose to demonstrate the devices in a top-contact configuration on Si/SiO_2 substrates. This bottom-gate approach makes photolithography challenging for top contacts above organic semiconductors, due to the developer and resist solvent chemistry. Inkjet printing could be used to pattern top contacts, although its limitations are the relatively restricted range of available conductive inks or precursors, as well as the sintering temperature for such inks, which could cause damage to underlying layers.

In the long term, inverting the device (bottom contact, top gate) would allow the use of the gate insulator to protect the active layer from, e.g., photolithography chemistry.

A complementary concern is the degradation of active layer or metal-semiconductor contact properties due to atmospheric exposure and ageing. While the fabricated devices showed good stability over 2.5 months of storage, it is likely that the more reactive, low work function metals required to create a barrier to the p-type semiconductor will see some evolution, modifying the contact profile. Notionally, a high-mobility p-type semiconductor with high ionization potential would be fairly stable to environmental exposure and would allow the use of higher work function metals to create a suitable, relatively low but reliable contact barrier. Au with suitable "barrier-raising" surface modification could be practical, but, as shown by the results of Cu/Au and Ni experiments, the transistors may not be operating fully in the SGT regime, reducing their utility, specifically, reducing drain current without decisively affecting saturation voltage.

Another practical aspect, which manifests with similar effects, is the composition of the gate stack. In this study, we have deliberately used a low-capacitance gate insulator to arrive at the low value for the saturation coefficient, which translates into low saturation voltage at the expense of increased gate-source voltage. It is entirely possible to realize OTFTs with much higher gate capacitance, but these would not have any of the benefits of OSGTs if rectifying contacts are used, due to the lack of saturation at the source ($\gamma \approx 1$). Practically, these transistors would behave as low drive voltage OTFTs with diminished drain current, unlikely to be practically superior in any application.

Naturally, the question arises as to the utility of SGT implementations in contrast with low-voltage TFTs with excellent performance in the conventional metrics. An example utilizes the lower transconductance of SGTs resulting from the injection control mechanism. A typical use case would be a display pixel driver[63] (voltage controlled constant current source), which operates at reasonably high current densities but at relatively low switching speeds. A lower transconductance (less steep transfer curve around and above threshold) would increase the range of the input (gate-source) voltage over the range of desired output currents, leading to better separation of the grey levels and more precise programming of individual pixels.[64] In addition, an SGT drive transistor's low saturation voltage reduces the power dissipation, as it allows a lower voltage power rail to be used. Moreover, the flat output curves also contribute to superior brightness uniformity across the display area, as the driver would be less affected by the I–R voltage drop, which occurs on the power rails in active matrix designs.[63]

We have also shown[65] that running a SGT at constant current in a diode connection allows a temperature-dependent voltage readout at the gate, which has a high swing between the power rails if γ is comparatively low.

Potentially highly stable and able to yield extremely low output conductance, such transistors should find numerous use cases in low-frequency analog applications. Perhaps more stimulating, the measurable reduction of the drain current with increasing temperature for these contact-controlled transistors

offers the prospect of implementing highly robust unipolar circuits with self-compensation functionality by using only a handful of transistors with complementary properties. Coupled with the simplicity of organic-TFT processing, the present findings may prove essential for the next decade of evolution in the flexible and printed electronics field.

5. Experimental Section

OTFT and OSGT Fabrication: Bottom-gate, top-contact OTFTs and OSGTs were fabricated in the inverted staggered device architecture on heavily doped silicon substrates. The gate dielectric is a stack of thermally grown silicon dioxide (100 nm thick), atomic-layer-deposited aluminium oxide (8 nm thick; deposited at a temperature of 250 °C), and a self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid ($C_{14}H_{29}PO(OH)_2$; PCI Synthesis, Newburyport, MA, USA).[61] The SAM was obtained by immersion of the substrate into a 2-propanol solution of phosphonic acid. Next, a 25-nm-thick layer of dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT, Sigma–Aldrich)[34] was deposited by thermal sublimation in vacuum, with the substrate temperature maintained at 60 °C and a deposition rate of 0.3 $Å s^{-1}$. Source/drain contacts were deposited by thermal evaporation in vacuum and patterned using a shadow mask, containing electrode arrays with a width $W = 200$ µm and varying channel lengths L (also referred to as source-drain separation d in OSGTs) ranging from $L = 20$ to 200 µm. The following metals were all evaporated in vacuum (at a rate of 0.3 $Å s^{-1}$) on different samples: 30 nm Au, 50/20 nm Ti/Au, 30/30 nm Cu/Au, 30 nm Ni. Due to metal deposition taking place in a single step issued from different boats, the second layer of Au is somewhat shifted (Figure 1a) and creates blurring.[62] This is not seen as an impediment to fabrication, as obtaining device operating behavior was the priority, rather than process optimization. As the blurring leads to shortening of the source-drain gap, optical measurements have been conducted to estimate the resultant dimensions, of which the effective reduction in d was ≈20 µm less than the shadow mask design. Oxidation at the edges might also contribute to discrepancies in d.

Device Storage and Preparation: Samples were stored in Ar to reduce effects of oxidation on exposed DNTT, except for the assessment of long-term exposure to air ambient (measurements repeated at 33 and 70 days later), where devices were stored in a dark cupboard over time. Prior to measurement, devices were individually isolated by scoring the DNTT around the contacts to reduce any fringe electric fields and reduce any gate leakage current, which may arise from the presence of a large, parasitic-gated semiconductor region (Figure 1h). The scoring resulted in highly irregular borders, thus device widths for TiAu and CuAu have been estimated to the nearest 10 µm. Hence, some values of drain current for these devices might not be representative of their true output, but considering the focus is on device behaviour, rather than performance, it was deemed adequate. A diamond scribe was used to expose the doped Si, which acted as a global back-gate.

Electrical Characterization: Measurements were taken using a Wentworth probe station connected to a Keysight B2902A source/measure unit (SMU) and temperature-controlled chuck (HC250). The majority of characterization was performed with the hot chuck set to 35 °C. A Hanna HI 8757 K-Type thermocouple (accuracy of +/- 0.5%) was used to measure sample temperatures. For the temperature study, measurements were taken from 35 to 75 °C in 10 °C steps. To account for nonlinearity in the hot-chuck control system, temperatures reported here were based on the readout from the Hanna thermocouple and have been converted to Kelvin. Hence, the measurements yield a higher degree of accuracy, even though the steps were no longer even. For light conditions, a Fiber-Lite 190 (high intensity cold light), fiber optic illuminator was used. Dark conditions were performed in the same room but with all lights turned off. The room was not completely dark, due to light from the door and equipment for taking measurements, however the condition was seen as adequate for assessing NDR.

LTPS SGT Fabrication: Comparison BGTC low temperature polycrystalline silicon SGTs with Cr Schottky contacts were fabricated according to Ref. [40] and included 200/200 nm SiO_2/SiN_x gate insulator stack and 35 nm active layer with dimensions $W = 10$ µm, $S = 8$ µm, $d = 10$ µm. Barrier height was tailored with a BF_2 barrier modification implant of $1{\cdot}10^{13}$ cm^{-2} (see Ref. [40] for additional details).

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

contact effects, organic semiconductors, source-gated transistors, temperature effects, thin-film transistors

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