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THM-OTFT: A Complete Physics-Based Verilog-A Compact Model for Short-Channel Organic Thin-Film Transistors

ALEXANDER KLOES [1] (Senior Member, IEEE), JAKOB LEISE [1,2], JAKOB PRUEFER [1,2], ARISTEIDIS NIKOLAOU [1,2], BENJAMÍN IÑÍGUEZ [2] (Fellow, IEEE), THOMAS GNEITING [3] (Senior Member, IEEE), HAGEN KLAUK [4], AND GHADER DARBANDY [1]

1 Compentence Center Nanoelectronics and Photonics, TH Mittelhessen-University of Applied Sciences, 35390 Giessen, Germany
2 Department of Electronic Engineering, Universitat Rovira i Virgili, 43007 Tarragona, Spain
3 AdMOS GmbH, 72636 Frickenhausen, Germany
4 Research Group Organic Electronics, Max Planck Institute for Solid State Research, 70569 Stuttgart, Germany

CORRESPONDING AUTHOR: A. KLOES (e-mail: alexander.kloes@ei.thm.de)

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ABSTRACT This paper presents a compact model for organic thin-film transistors fabricated in the staggered or coplanar device architecture which includes short-channel effects related to the potential barrier in the channel region, which manifest themselves as threshold voltage roll-off, drain-induced barrier lowering, and subthreshold swing degradation. Furthermore, the effect of non-linear injection due to a work-function mismatch between the source/drain contacts and the semiconductor is considered. The model includes a charge-based capacitance model considering overlap and fringing regions in short-channel multi-finger layout structures. Extensions include a model for drain-current variability, low-frequency noise and non-quasistatic effects. The introduction of physically meaningful fitting parameters provides a high degree of flexibility to the model. The equation package is verified using the results of measurements performed on transistors fabricated on flexible substrates and is available in Verilog-A for an efficient circuit simulation on different design platforms.

INDEX TERMS Organic semiconductor, thin-film transistor, compact model, device modeling, short channel, capacitance, variability, noise.

I. INTRODUCTION

Organic thin-film transistors (OTFT) have evolved as candidates for large-area flexible electronics, as they can typically be fabricated at low temperatures compatible with polymeric substrates. Envisaged applications range from wearable electronics to display backplanes [1], [2]. Recent advances in device technology have pushed the maximum operational frequency well into the megahertz regime [3].

The design of complex integrated systems based on organic transistors relies on accurate and efficient compact models for these devices, serving as a bridge between device technology and the circuit level and allowing for efficient circuit simulation. Based on the physics of organic semiconductors (OSC) [4], [5], numerous approaches to compact models for organic TFTs have been proposed [6], [7]. However, some of them are lacking physical insight or do not provide the flexibility required for the model to be readily adapted to different technologies. Moreover, most compact models are not suitable for both DC and AC circuit simulations. In other words, a standard compact model dedicated to the physics and the static and dynamic behavior of OTFTs is still lacking, despite the fact that such a model is a prerequisite for establishing an effective collaboration between fabless design houses and foundries.

In this paper, we present a complete physics-based compact model for OTFTs fabricated in the staggered or the coplanar device architecture (refer to Fig. 1). The DC model is able to capture the effects of small channel lengths on the potential barrier and of non-linear contact characteristics [8]. The AC model uses the same charge expressions as the DC model, considers fringing capacitances in multi-finger structures and includes non-quasistatic effects. Furthermore, a model for low-frequency noise (LFN) has been implemented. Although some parts of the model have already been published, this paper for the first time presents an overview of the complete compact model (including the parameters relevant for the interface to a Verilog-A implementation), explains the interdependencies between the different modules, and provides guidelines for parameter extraction.

The paper is organized as follows. Section II reviews the core DC model and its basic expressions for the accumulated channel charge which are fundamental for the whole model. All model extensions related to short-channel effects, non-linear contact resistance, fringing effects, and the DC variability due to a fluctuation of the channel current are summarized. Hereby, the summary of the model parameters provided in Table 1 serves as a reference for the interface to the model. After comparing the DC model to measurement results, Section III summarizes the capacitance model, including fringing effects, non-quasistatic effects and LFN. Again, verification results are also shown. Finally, guidelines for a parameter extraction for the Verilog-A implementation of the model are given in Section IV, and Section V gives conclusions.

II. DC MODEL

The core DC model is an expression for the current in long-channel devices. Because its equations are fundamental to the entire compact model, they will be briefly reviewed in the next section. After that, model parameters such as threshold voltage and subthreshold swing are replaced by expressions accounting for short-channel effects. Non-linear effects at the source and drain junctions are considered by an additional contact resistance that degrades the effective carrier mobility in the model. Finally, current fringing effects in a multi-finger layout are taken into account, and an extension for evaluating the drain-current variability is introduced.

A. LONG-CHANNEL CURRENT MODEL

The DC model for the intrinsic transistor has been derived from a single expression for the accumulated channel charge which is valid from below to above-threshold operation [9]. The result is a continuous expression for all regions of operation, without further artificial smoothing. The Gaussian density of states (DOS) in organic semiconductors is included by an empirical power-law mobility expression.

The DC model in [7], [9] is a charge-based model, which means that the current is calculated based on the charge densities Q'_{ms} and Q'_{md} on the source and the drain ends of the channel (see Fig. 1). These charge densities are calculated as follows:

$$Q'_{\mathrm{ms/d}} = \frac{S}{\ln(10)} \cdot C'_{\mathrm{ox}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\mathrm{gs/d}} - V_{\mathrm{T0}}}{S/\ln(10)}\right)\right\}, \tag{1}$$

where $\mathcal{L}$ is the first branch of the Lambert W function, C'_{ox} is the capacitance of the gate dielectric per gate area, S is the subthreshold swing, and V_{T0} is the threshold voltage. The model takes into account the hopping transport together with the effect of the Gaussian DOS by a field-dependent mobility [10]:

$$\mu = \kappa \cdot \left(\frac{Q'_{\mathrm{ms}}}{C'_{\mathrm{ox}}}\right)^{\beta}, \tag{2}$$

where κ [$\mathrm{cm^2V^{\beta-1}s^{-1}}$] is a proportionality factor and β is the power-law factor. An ohmic contact resistance (R_{contact}) and a possible non-linear resistance (R_{sb}) at the source-to-channel Schottky barrier due to a work-function mismatch are taken into account by introducing an effective mobility:

$$\mu_{\mathrm{eff}} = \frac{\mu}{1 + \mu \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot (R_{\mathrm{contact}} + R_{\mathrm{sb}}) \cdot Q'_{\mathrm{ms}}}. \tag{3}$$

Finally, the drain current reads as follows:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot \left(\frac{k_{\mathrm{B}} \cdot T}{q} \cdot \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md}}}{L_{\mathrm{ch}}} + \frac{Q'^2_{\mathrm{ms}} - Q'^2_{\mathrm{md}}}{2 \cdot L_{\mathrm{ch}} \cdot C'_{\mathrm{ox}}}\right) \times (1 + \lambda \cdot (V_{\mathrm{ds}} - V_{\mathrm{dsx}})), \tag{4}$$

where L_{ch} and $W_{\mathrm{ch,eff}}$ are the channel length and the effective width. The parameter λ is the channel-length modulation factor. The effective drain-source voltage V_{dsx} tends to the

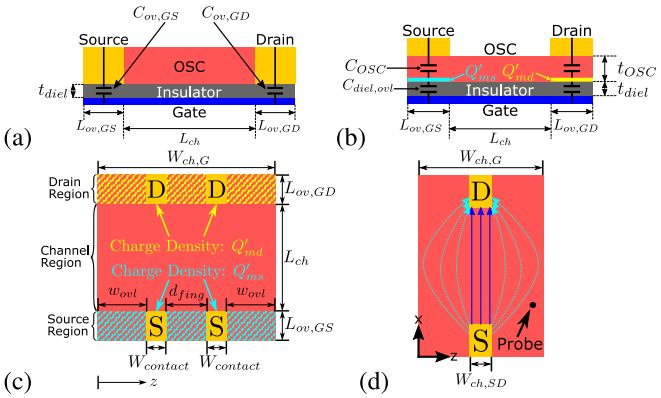

FIGURE 1. Schematic cross section of OTFTs in the (a) bottom-gate, bottom-contact (BC; coplanar) and (b) bottom-gate, top-contact (TC; staggered) device architecture. (c) Schematic top view of a BC TFT close to the gate dielectric surface. For the compact model, it is assumed that the charge density in the source (drain) region is equal to the charge density at the source (drain) end of the channel [15], [21]. (d) Schematic of the current flowing in a planar OTFT. If there are fringing regions, the current not only flows directly from source to drain, but also in the fringing regions (dotted arrows). As the paths through the fringing regions are longer, the current density in the fringing regions is smaller than in the center of the channel. At the probe point, the current density is assumed to be low. However, the density of accumulated quasi-mobile charges is assumed to be the same as in the center of the channel.

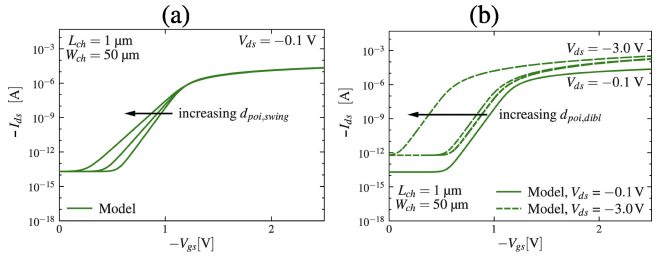

FIGURE 2. Influence of short-channel model parameters on the transfer characteristics of an OTFT. Parameter d_{poi} is the "point of interest" in the calculation of the potential barrier height in the channel region. Its value depends on whether the OTFT is operated (a) below the threshold voltage (in which case the most conductive path is located some distance away from the dielectric interface, and d_{poi} defines the subthreshold swing), or (b) above the threshold voltage (in which case the accumulation channel is formed close to the dielectric interface, and d_{poi} is used to calculate the threshold voltage or the drain-induced barrier lowering, DIBL).

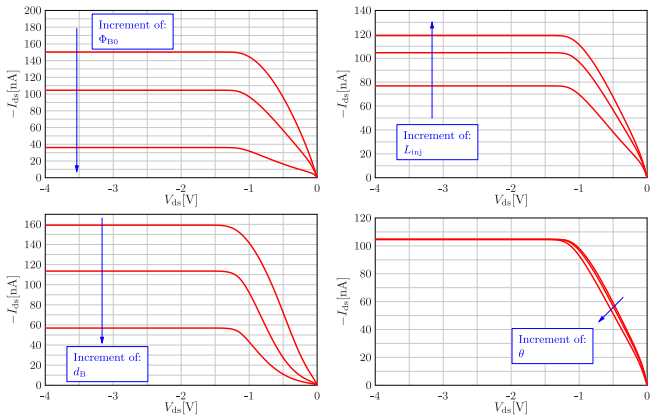

FIGURE 3. Influence of four different parameters that are part of the Schottky-barrier contact model on the DC output characteristics of OTFTs. The source-related parameters Φ_{B0}, L_{inj} and d_B are the Schottky barrier height, the injection length (approximately the gate-to-contact overlap length in staggered transistors, or the thickness of the accumulation channel in coplanar OTFTs), and the distance of the point of injection from the interface to the gate dielectric, respectively. The parameter θ helps to adapt the curve considering an additional voltage drop across the Schottky barrier at the drain.

saturation voltage V_{dsat} in the saturation regime and is given by

$$V_{\mathrm{dsx}} = \frac{1}{C'_{\mathrm{ox}}} \cdot \left(Q'_{\mathrm{ms}} - Q'_{\mathrm{md}}\right). \tag{5}$$

B. SHORT-CHANNEL EFFECTS

If the channel length is small (a few micrometers or less), the OTFT's current-voltage characteristics are likely dominated by short-channel effects, similar to those known from silicon transistors. The impact of the source/drain potentials on the potential barrier in the channel region will typically result in a threshold voltage shift (VT roll-off), drain-induced barrier lowering effects (DIBL), and a degradation of the subthreshold swing. In order to incorporate these effects in the model, a two-dimensional solution of the potential in the channel region has been developed, from which closed-form expressions for the aforementioned effects have been derived. The model provides solutions for the staggered and the coplanar device architectures [11], [12], [13]. It has been shown that for each of the short-channel effects, the potential solution must be calculated for various distances from the gate dielectric (d_{poi}). Therefore, three model parameters controlling these short-channel effects separately were introduced. Their impact on an OTFT transfer characteristics is shown in Fig. 2. Please note that in this way, the model is scalable, i.e., there is only one model card for devices with various channel lengths.

C. CONTACT RESISTANCE

Due to the lowering of the channel resistance in short-channel devices, the current limitation imposed by the source and drain contacts becomes more dominant. If the mismatch between the work function of the contact material and the organic semiconductor is relatively large and cannot be neglected, in addition to the ohmic contact resistance the effect of non-linear current injection can be visible in the transistor's output characteristics.

In our model, the current injection at the source contact through the reverse-biased Schottky barrier is calculated from the effective electric field at the point of injection [13], [14]. In view of numerical efficiency, the current-limiting behavior is converted into an equivalent bias-dependent resistance R_{sb}, which is incorporated into the intrinsic transistor model by using equation (3) for the effective mobility. The forward-biased drain barrier is taken into account by an additional voltage drop $V_{\mathrm{sb,d}}$. This is done by one iteration: first, equations (1) to (4) are computed without the voltage drop. From this result, $V_{\mathrm{sb,d}}$ is calculated. Finally, the charge density at the drain side is calculated again, but this time taking into account the voltage drop $V_{\mathrm{sb,d}}$, and from (4), the DC current is obtained.

Fig. 3 illustrates the flexibility of the model to capture the s-shape of the output characteristics by using different physically meaningful fitting parameters.

D. FRINGING EFFECTS

The fringing regions open additional paths for the current; this can be viewed as a current spreading. However, the current density in the fringing regions will be smaller than in the channel, especially in regions far away from the channel center, due to the weaker electric field. The current spreading is schematically shown in Fig. 1d. The behavior is modeled as a change in the effective channel width $W_{\mathrm{ch,eff}}$ for the current [15], [16].

To account for the fringing effects, the drain current given by (4) is modified. It is assumed that the effective channel width is larger than the width of the contacts ($N_{\mathrm{fing}} \cdot W_{\mathrm{contact}}$), but smaller than the width of the gated semiconductor $W_{\mathrm{ch,G}}$ (refer to Fig. 1d). Note that the width $W_{\mathrm{ch,G}}$ includes both the fringing regions outside the outermost contact fingers (w_{ovl}) and the fringing regions between the contact fingers. The effective gate width is defined as follows:

$$W_{\mathrm{ch,eff}} = \delta_{\mathrm{fit}} \cdot W_{\mathrm{ch,G}} + (1 - \delta_{\mathrm{fit}}) \cdot N_{\mathrm{fing}} \cdot W_{\mathrm{contact}}, \quad (6)$$

where N_{fing} is the number of fingers, and d_{fing} is the distance between the fingers. The fitting parameter $\delta_{\mathrm{fit}} \in [0, 1]$ is assumed to be bias-independent [15].

E. DRAIN-CURRENT VARIABILITY

Drain-current variability can be perceived as the time-independent variation of the drain current of two or more nominally identical transistors under the same biasing conditions. Here, the device-level charge-based variability model from [17] is used. The proposed physical model has two fitting parameters, can be applied directly to the experimental statistical population without the need for Monte Carlo simulations and accurately describes the bias-dependent variability of organic TFTs, fabricated either in the staggered or the coplanar device architecture.

The model parameter $N'_{\mathrm{t,var}}$ denotes the density of charges being trapped in the channel region per gate area, which cause a local fluctuation of the accumulated charge density in the channel. The parameter α^* is related to Coulomb scattering induced by the trapped charges that manifests itself as a reduction of the effective carrier mobility in the channel. However, it should be noted that because of the factor $\mu_{\mathrm{eff}} W_{\mathrm{ch,\,eff}}/L_{\mathrm{ch}}$ in (4), in the current-voltage characteristics, this charge-carrier-correlated mobility fluctuation cannot be distinguished from edge effects [18].

If the drain-current variability model is switched on (model parameter var_mod=1), the calculated drain current is equal to its mean value plus or minus a multiple of its standard deviation σ, depending on the model parameters sigma_sign and sigma_factor.

F. RESULTS

Results obtained using the DC model in comparison to results of measurements performed on coplanar OTFTs with a channel length of 1 µm are shown in Fig. 4. The devices were fabricated on flexible PEN substrates using stencil lithography [19]. The gate electrodes are vacuum-deposited aluminum, the gate dielectric consists of plasma-grown aluminum oxide and a self-assembled monolayer (*n*-tetradecylphosphonic acid) with a total thickness of 9 nm, the source and drain contacts are vacuum-deposited gold with a thickness of 30 nm, and the OSC is vacuum-deposited DPh-DNTT with a nominal thickness of 20 nm. Results obtained using the variability model are shown in Fig. 4d. For further verification of the DC model, including for OTFTs fabricated in the staggered device architecture, please refer to [11], [12], [14].

III. AC MODEL

From the DC model described in Section II, a quasistatic AC model has been derived. The model accounts for the intrinsic channel charges, parasitic charges in the overlap regions and for charges in the fringing regions (in OTFTs with a multi-finger structure) [15], [16].

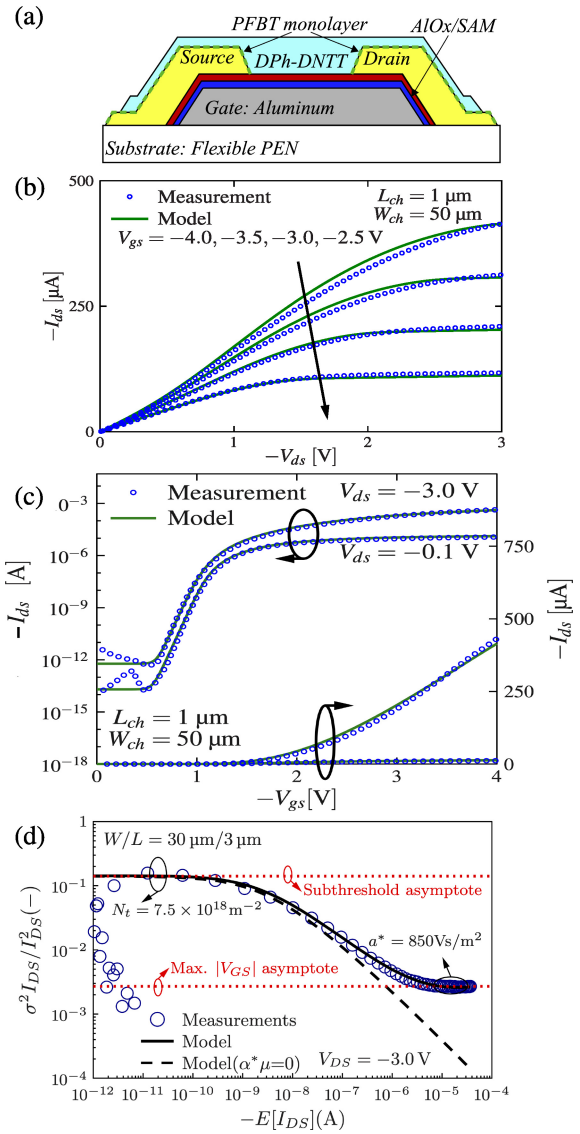

FIGURE 4. (a) Schematic cross section of DPh-DNTT TFTs fabricated in the coplanar device architecture [19]. (b) Output and (c) transfer characteristics calculated using the compact model including short-channel effects and non-linear injection at the contacts, compared with results of measurements performed on a device with a channel length of 1 μm. (d) Normalized drain-current variance $\sigma^2 I_{DS}/I_{DS}^2$ versus mean-value drain current $E[I_{DS}]$ for OTFTs with $L_{ch} = 3$ μm. The experimental mean values were calculated over a population of 16 nominally identical transistors [17].

A. INTRINSIC CAPACITANCES

The intrinsic charges are calculated by integrating the charge density per gate area of the DC model along the channel, which leads to a closed-form equation for the total channel charge. Applying the well-known Ward-Dutton partitioning scheme [20], the channel charges are separated into parts attributed to the source or the drain terminal.

As a result, these charge equations are valid only for transistors that exhibit zero or negligibly small (with respect to the channel resistance) contact resistances. However, contact effects also have an influence on the capacitances, especially

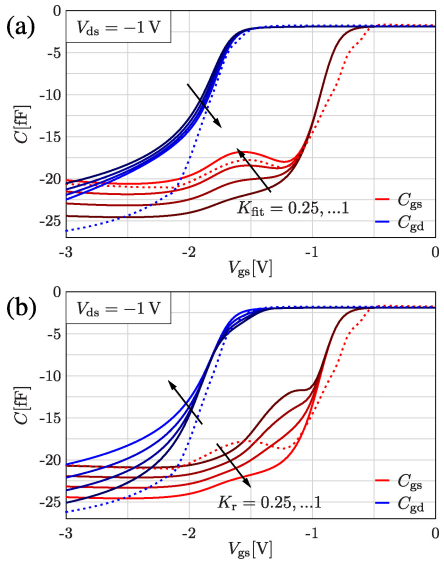

FIGURE 5. Voltage dependence of the quasistatic capacitances C_{gs} and C_{gd} of staggered short-channel OTFTs ($L_{ch} = 2\mu$m) at $V_{ds} = -1$V. The results from the compact model (solid lines) are compared to results from a TCAD Sentaurus simulation (dotted lines). The curves demonstrate the effect of the fitting parameters (a) K_{fit} and (b) K_r.

if the contact resistances are high in comparison to the intrinsic channel resistance. In the DC model, the contact resistances $R_{contact}$ and R_{sb} are calculated. For simplicity and numerical performance of the DC model, these resistances are not introduced as lumped elements. Instead, as explained in Section II-C, they lower the effective mobility of the charge carriers in the channel. So while these elements provide an accurate prediction of the current-voltage characteristics of the OTFTs, they cannot necessarily be used to obtain an accurate estimation of the voltage drops at the contacts. To be able to incorporate the voltage drops at the Schottky barriers into a short-channel capacitance model, the parameters K_{fit} and K_r have been introduced [16], [21]. They make it possible to adapt the characteristics of the internodal capacitances by modifying the weight of the contact resistances and their distribution between the source contact and the drain contact. Furthermore, the parameter ν allows a fine tuning of the Ward-Dutton charge partitioning.

Figure 5 demonstrates how the voltage dependence of the capacitances C_{gs} and C_{gd} of staggered short-channel OTFTs is affected by the model parameters K_{fit} and K_r. Numerical results obtained using TCAD Sentaurus [22] are shown as a reference.

B. EXTRINSIC CAPACITANCES

The density of intrinsic charges is calculated in the same manner for staggered and coplanar transistors. However, as illustrated in Fig. 1a and b, due to the overlap regions, there are fundamental differences between the densities of extrinsic charges in the two OTFT architectures. In coplanar transistors, the source/drain contacts are separated from the gate electrode only by the gate dielectric; an arrangement that can be approximated by simple plate capacitors. In contrast, in staggered transistors, the source/drain contacts are separated from the gate electrode by a stack consisting of the organic semiconductor and the gate dielectric. For this series connection of two capacitors, additionally the same density of accumulated charges given by the DC model for the source end (Q'_{ms}) and the drain end (Q'_{md}) of the channel is being considered. This results in a bias-dependent charge model, as presented in [15], [16].

Additionally, in a multi-finger layout, as depicted in Fig. 1c, all charges in the fringing regions have to be considered. In our model, we assume that for both staggered and coplanar devices, the charge density per gate area in the source region (hatched region in Fig. 1c, which excludes the areas of direct overlap between gate electrode and the source/drain contacts) is equal to the density of accumulated charges Q'_{ms} and Q'_{md} at the source/drain ends of the channel. This has been confirmed by numerical TCAD Sentaurus simulations, and these additional charges are a substantial contribution to the total extrinsic capacitances [16], [21]. In this way, in our model we are taking into account the layout of the OTFT. Therefore, our capacitance model goes beyond a simple two-dimensional modeling approach derived from the device cross section alone. The increase of the active area according to the layout of the multi-finger structure is necessary for obtaining a good agreement between the small-signal gain calculated using the compact model and the result derived from measurements [21].

C. NON-QUASISTATIC EFFECTS

The quasistatic small-signal model of the transistor considers capacitances as lumped elements between the device contacts. However, the accumulated charge is distributed along the channel, and therefore with increasing frequency, the channel starts to behave as an RC delay line, with a capacitance distributed along the channel resistance. Furthermore, charge trapping in the gate dielectric or the semiconductor has an additional impact on the formation of the intrinsic charges. These effects cannot accurately be captured by a quasistatic charge calculation as proposed in the previous section. In the literature, sophisticated non-quasistatic approaches have been proposed [23]. However, in our model we follow an empirical approach from [24]. Here, the quasistatic capacitances are multiplied by a scaling function, modifying the lumped elements depending on the empirical model parameters τ_{scale} and p_{scale}:

$$C_{scale} = C_{scale,high} + \frac{C_{scale,low} - C_{scale,high}}{(1 + f \cdot \tau_{scale})^{p_{scale}}}. \quad (7)$$

Since the frequency f is not available within the Verilog-A environment during runtime of an AC analysis, this scaling factor has to be calculated prior to the simulation for the frequency of interest, and its value has to be provided as an input parameter to the compact model. The Verilog-A implementation of our model makes it possible to apply this approach separately for the scaling of the quasistatic

extrinsic and intrinsic capacitances, which during runtime are multiplied by the model parameters C_{scale} and C_{scale2}, respectively [16], [21].

D. LOW-FREQUENCY NOISE

The model takes into account two discrete sources for LFN in organic TFTs. One is the noise due to the carrier-number and correlated mobility-fluctuation effect (ΔN noise), which originates from local random fluctuations of the carrier density due to trapped charges, additionally causing correlated Coulomb scattering [25]. The other is the noise due to the fluctuation of the charge-carrier mobility ($\Delta\mu$ noise) [26].

The model equations have been derived following the methodology in [27], in our case starting from the charge density given by equation (1) of the DC model, leading to expressions combining the ΔN and $\Delta\mu$ noise [28]. The influence of the model parameters σ, N_{t}', λ_{tun} and α_{c} on the noise power spectral density (PSD) is illustrated in Fig. 6a-c.

E. RESULTS

In Fig. 6d, results of the LFN model are shown in comparison to noise measurements performed on staggered OTFTs. Fig. 7a and b show model results for the internodal intrinsic capacitances in a short-channel OTFT compared to results of TCAD Sentaurus simulations, allowing for a verification with defined structural and material parameters [15]. The fitting of the model provides an overall good agreement between model and simulations. However, a compromise has to be made regarding the voltage dependence of C_{gs} and C_{sg} at the transition from the linear to the saturation region, which is due to the consideration of the voltage drops at the contacts by an effective mobility in the DC model (for sake of numerical efficiency), which can only to a certain degree be compensated for by the model parameters K_{fit}, K_{r} and ν in the capacitance model. Fig. 7 shows a verification of the model by comparison to measurements performed on staggered and coplanar OTFTs having a channel length of 0.67 µm and a variation of the gate-to-source and gate-to-drain overlaps. The model is able to capture the degradation of the small-signal gain up to frequencies of several megahertz and correctly predicts the higher transit frequencies of coplanar devices [21].

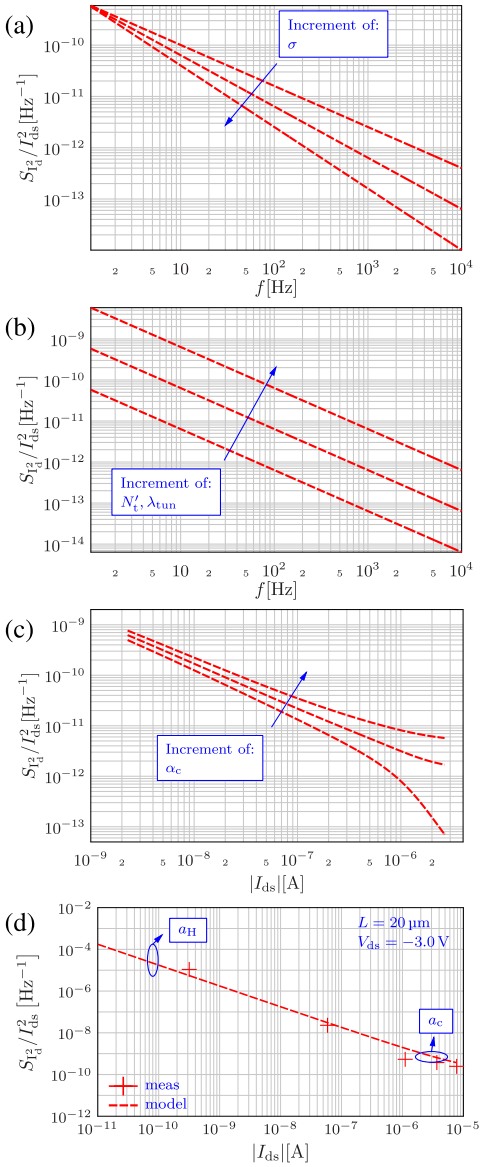

FIGURE 6. Influence of the parameters of the model for the LFN on the noise power spectral density (PSD). (a) PSD versus frequency with variation of the exponent in the $1/f^{\sigma}$ behavior. (b) PSD versus frequency with variation of the parameter N_{t}'. (c) PSD versus drain current at a fixed drain-source voltage and a fixed frequency at which the parameter α_{c} is varied. (d) The LFN model compared to noise measurements performed on staggered OTFTs (averaged over 15 devices with $L = 20$ µm and $W = 100$ µm). The $\Delta\mu$ noise dominates at lower currents, controlled in the model via parameter α_{H}. At higher currents, LFN is due to ΔN noise. In this regime, the model is fitted by parameter α_{c} to measurements [28].

IV. PARAMETER EXTRACTION

In the derivation of the equation package for the compact model, a physics-based approach that considers two-dimensional effects has been followed. As a result, the compact model demonstrates a good scalability and makes it possible to define one parameter set covering devices with a range of layout dimensions. Nevertheless, to obtain a perfect fit for OTFTs with a wide range of channel lengths, several fitting parameters must be adjusted. This is not only due to approximations introduced in the modeling approach, but also due to the fact that the fabrication process of OTFTs introduces an additional variability to the model parameters which are taken as global parameters for the semiconductor. The morphology of the OSC layer is expected to be different in the close vicinity of the source and drain contacts, which has an impact on the local mobility, trap density, contact resistance and non-linear injection. These effects are particularly pronounced in short-channel devices, making an adaption or binning of related model parameters necessary.

A Verilog-A implementation of the equation package is provided by [29]. It should be noted that the code includes an option for the separation of the device channel into a number

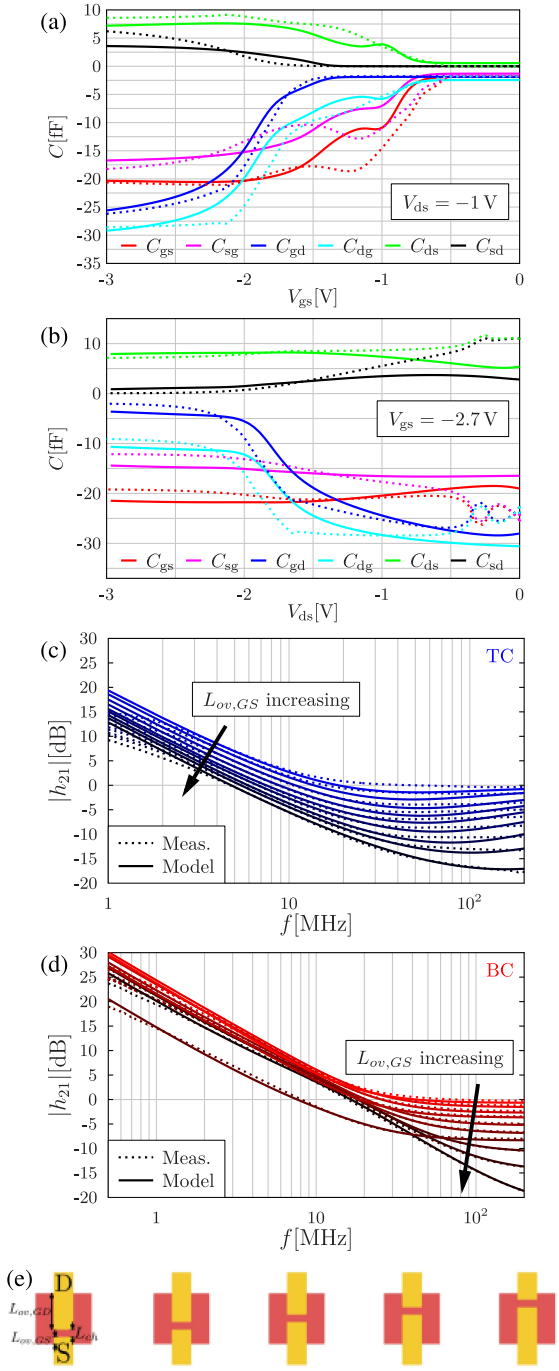

FIGURE 7. Voltage dependence of the quasistatic capacitances of a short-channel staggered OTFT ($L_{ch} = 2\mu$m) at (a) $V_{ds} = -1$ V and (b) $V_{gs} = -2.7$ v. Compact model: solid lines, TCAD Sentaurus simulations: dotted lines. The parameters of the capacitance model are chosen as follows: $K_r = 0.15$, $K_{fit} = 0.24$, and $\nu = 0.3$. (c) Small-signal gain (h_{21}) of staggered (bottom-gate, top-contact; TC) and (d) coplanar (bottom-gate, bottom-contact, BC) OTFTs with $L_{ch} = 0.67\mu$m and asymmetric gate-to-source and gate-to-drain overlaps at $V_{gs} = V_{ds} = -3$ *textV* [21]. Model: solid lines, measurements: dotted lines. The pictogram in (e) shows the asymmetry with a constant total overlap $L_{ov,GS} + L_{ov,GD} = 10\mu$m for the measured devices.

of discrete segments [27], allowing for a more precise simulation of non-quasistatic effects. For details, please refer to [29]. Furthermore, the temperature dependence of the DC model in the range of temperatures from 300 to 340 K has been investigated in [16], and empirical expressions for a shift of the threshold voltage and a drift of the effective mobility have been proposed.

In the following, the main steps for arriving at a set of model parameters (refer to Table 1) for the Verilog-A implementation without channel segmentation are summarized. For more details, including a step-by-step illustration, refer to [29]. It should be noted that some model parameters show mutual dependencies, and therefore a tool for global parameter extraction is beneficial.

For circuit simulation results demonstrating the numerical stability and convergence of the model, please refer to [15] where several input decks, model cards and data from measurements or TCAD simulations are provided for benchmarking.

A. DC MODEL

A.1. LONG-CHANNEL OTFTs

First, the structural and material parameters are set to the best knowledge to their physical values. With all short-channel models switched off (Schottky-barrier models, subthreshold-swing degradation, threshold-voltage roll-off, DIBL effect), the DC parameters for mobility, threshold voltage and subthreshold swing are adapted to obtain a good fitting to the measured transfer and output characteristics of the device with the largest channel length. If devices in a multi-finger layout with varying numbers of fingers or varying finger width are available, this will make it possible to extract the current-fringing parameter δ_{fit}.

A.2. SHORT-CHANNEL OTFTs

The short-channel model extensions related to threshold-voltage roll-off, DIBL and subthreshold-swing degradation are switched on. The corresponding model parameters are adapted to obtain a good agreement between model and measurement data when these effects are visible in the transfer characteristics of short-channel OTFTs. The physically meaningful values $d_{poi,swing} = d_{poi,dibl} = t_{diel}$ and $d_{poi,rolloff} = t_{diel} + t_{osc}$ (and in the case of coplanar OTFTs: $q_{co} = 1$) can be used as a starting point. Next, focusing on the output characteristics, the ohmic contact resistance $R_{contact}$ is adjusted together with the power-law mobility factor β.

If the output characteristics show a region of non-linearity in the linear operation region, the Schottky-barrier models must be enabled. By simultaneously adapting all related parameters, the shape of the non-linear region is adapted. Please note that the non-linear injection model has an impact on the effective mobility in the channel. Therefore, any modification of the model parameters for non-linear injection makes it necessary to readjust the mobility parameters. Finally, a reinspection of devices with different channel lengths reveals for which model parameters a binning is necessary, resulting in slightly different model cards depending on the channel length.

TABLE 1. Verilog-A model parameters.

Symbol	Values	Description
	(Figs. 4b and c)	*Material parameters*
$\varepsilon_{\mathrm{diel}}$	8	Relative dielectric permittivity of gate dielectric
$\varepsilon_{\mathrm{osc}}$	3	Relative dielectric permittivity of OSC
χ_{osc}	$1.81\,\mathrm{eV}$	Electron affinity of OSC
E_{HOMO}	$5.19\,\mathrm{eV}$	HOMO level of OSC
$\Phi_{\mathrm{m,sd}}$	$4.65\,\mathrm{eV}$	Work function of the source/drain electrodes
		Structural parameters
$type\_$	-1	1: n-type, -1: p-type
$structure$	1	0: staggered, 1: coplanar
L_{ch}	$1/1.4/2.4/4.5/10.5\mu m$	Channel length
W_{contact}	$50\,\mu\mathrm{m}$	Electrode width of one S/D finger
t_{diel}	$8\,\mathrm{nm}$	Thickness of the gate dielectric
t_{osc}	$25\,\mathrm{nm}$	Thickness of the OSC
$L_{\mathrm{ov,GS}}$	$10\,\mu\mathrm{m}$	Overlap between the source electrode and the gate
$L_{\mathrm{ov,GD}}$	$10\,\mu\mathrm{m}$	Overlap between the drain electrode and the gate
w_{ovl}	0	Length of fringe regions beyond first and last finger
N_{fing}	1	Number of fingers
d_{fing}	0	Distance between each S/D finger
L_{ext}	0	Extended overlap (staggered)
		DC fitting parameters
κ	$6.7\,\mathrm{cm}^2\mathrm{V}^{-\beta-1}\mathrm{s}^{-1}$	Low field mobility
β	0.65	Power law factor
V_{T0}	$-1.06\,\mathrm{V}$	Threshold voltage
S_{obs}	$0.08\,\mathrm{V/dec}$	Inverse subthreshold slope
λ	0	Channel length modulation factor
$R_{\mathrm{leak,ds}}$	$5\cdot10^{12}\Omega$	Leakage resistance drain to source
$R_{\mathrm{leak,sg}}$	$10^{60}\Omega$	Leakage resistance source to gate
$R_{\mathrm{leak,dg}}$	$10^{60}\Omega$	Leakage resistance drain to gate
R_{sheet}	0	Sheet resistance of OSC (staggered)
L_{t}	0	Transfer length in contact regions (staggered)
R_{contact}	$2.42/3.15/5/8.2/15.5\mathrm{k}\Omega$	Ohmic contact resistance (coplanar)
δ_{fit}	1	Current fringing parameter $(0\ldots1)$
		Non-linear injection and short channel effects
SBdrain	1	Schottky barrier model for drain: on (1), off (0)
SBsource	1	Schottky barrier model for source: on (1), off (0)
d_{m}	$2\,\mathrm{nm}$	Thickness of the accumulation channel
d_{B}	$1.92\,\mathrm{nm}$	Fitting parameter of injection model
η	1.85	Non-ideality factor of SB thermionic emission current
θ	5	Non-ideality factor of SB diode
w_{sat}	5	Fitting parameter of drain SB model
SC_SubSwing	1	Subthreshold swing degradation: on (1), off (0)
SC_VTrolloff	1	Threshold voltage roll-off: on (1), off (0)
SC_DIBL	1	Drain-induced barrier lowering: on (1), off (0)
$d_{\mathrm{poi,swing}}$	$28.3\,\mathrm{nm}$	Fitting parameter for slope degradation ($\approx t_{\mathrm{diel}}+t_{\mathrm{osc}}$)
$d_{\mathrm{poi,rolloff}}$	$3.4\,\mathrm{nm}$	Fitting parameter for V_T roll-off ($\approx t_{\mathrm{diel}}$)
$d_{\mathrm{poi,dibl}}$	$28.3\,\mathrm{nm}$	Fitting parameter of DIBL model ($\approx t_{\mathrm{diel}}+t_{\mathrm{osc}}$)
q_{co}	0.999	Parameter defining contact thickness (coplanar) $(0\ldots1)$
		Capacitance model
K_{fit}	1	Fitting parameter for short-channel $(0\ldots1)$
K_{r}	0	Fitting parameter for short-channel $(0\ldots1)$
C_{scale}	1	Frequency dispersion of fringe charges $(0\ldots1)$
C_{scale2}	1	Frequency dispersion of intrinsic charges $(0\ldots1)$
ν	0	Parameter for charge partitioning (short channel) $(0\ldots1)$
	(Fig. 6d)	*Noise model*
λ_{tun}	$0.1\,\mathrm{nm}$	Tunneling attenuation distance
N_{t}'	$1.3\,10^{10}\mathrm{cm}^{-3}$	Density of traps per energy and volume
α_{c}	$5.97\,\mathrm{V/A}$	Coulomb scattering coefficient
σ	1	Exponent of the frequency in LFN model
α_{H}	$7.8\,10^{-3}$	Empirical Hooge parameter
	(Fig. 4d)	*Variability model*
var_mod	0	Variability model: on (1), off (0)
$N_{\mathrm{t,var}}'$	$7.5\,10^{-18}\mathrm{cm}^{-2}$	Density of traps per energy
$\alpha^\star$	$850\,\mathrm{Vs/m}^2$	Coulomb coefficient for correlated mobility fluctuation
sigma_sign	1	0/1: current at -sigma/+sigma
sigma_factor	0	Multiplication factor for the standard deviation sigma

The extracted values for the model parameters from the plots in Fig. 4b and c are shown in the Appendix, Table 1. In this case, the only model parameter which has to be adapted for channel lengths from 1 μm to 10.5 μm is the ohmic contact resistance [14].

A.3. VARIABILITY

Figure 4d illustrates how the model parameters for the drain-current variability can be extracted from a plot of the normalized drain-current variance $\sigma^2 I_{\mathrm{ds}}/I_{\mathrm{ds}}^2$ as a function of the mean-value drain current $E[I_{\mathrm{ds}}]$. In a first step, the

parameter α^* is set to zero. In the subthreshold region, (i.e., above the leakage-current regime), a specific gate-source voltage is selected, and $N'_{t,var}$ at this gate-source voltage is calculated. Black dashed lines show the results of the model without the mobility-fluctuation effect ($\alpha^* = 0$). In a second step, using the extracted value of $N'_{t,var}$, the parameter α^* is calculated at the maximum gate-source voltage. Note that the two selected gate-source voltages (subthreshold region and maximum $|V_{gs}|$) correspond to specific experimental values of $\sigma^2 I_{ds}/I_{ds}^2$ that define the subthreshold and maximum-$|V_{gs}|$ asymptotes that are depicted in Fig. 4d as red dashed lines. Extracted values for the model parameters are shown in the Appendix, Table 1.

B. AC MODEL

B.1. LONG-CHANNEL OTFTs

The AC model for long-channel devices during low-frequency operation does not require further fitting, because the charge-based capacitance model uses the same charge expressions as the DC model. Parameters controlling non-quasistatic effects must be set to $C_{scale2} = C_{scale} = 1$.

B.2. SHORT-CHANNEL OTFTs

By comparing the model to low-frequency measurements of the internodal capacitances in short-channel transistors, the corresponding fitting parameters are adapted. Setting of $K_{fit} = 1$, $K_r = 1$ and $\nu = 0$ is used as a starting point [15].

B.3. NON-QUASISTATIC EFFECTS

From capacitance measurements performed at high frequencies, the model may be adapted by decreasing the values of C_{scale2} and C_{scale}, thus making it possible to extract proper values for the parameters τ_{scale} and p_{scale} in equation (7). As noted in Section III-C, values of C_{scale2} and C_{scale} have to be provided externally to an AC simulation according to the frequency of interest.

B.4. NOISE

Noise parameters are extracted from plots of the power spectral density (PSD) versus the frequency (σ) and versus the drain current (λ_{tun}, N'_t) (refer to Fig. 6). From the above-threshold characteristics, the Coulomb scattering coefficient α_c is extracted, whereas the Hooge parameter α_H is adapted for the subthreshold region [28]. Table 1 in the Appendix gives the extracted values for the model parameters.

V. CONCLUSION

The presented compact model for OTFTs fabricated in the staggered or the coplanar device architecture presented here provides great flexibility to capture typical effects related to a small channel length or non-linear injection at the contacts. Additionally, the model includes expressions for the intrinsic and extrinsic charges in the devices, allowing for AC and transient circuit simulations. Extensions allow for an estimation of the drain-current variability and low-frequency noise. Its accuracy has been demonstrated by comparison to measurements performed on OTFTs with submicron channel lengths. The equation package has been implemented in Verilog-A and is available in [29] for circuit design, simulation and optimization to advance the integration of OTFTs into more complex systems.

APPENDIX

See Table 1.

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