Unipolar Circuits Based on Individual-Carbon-Nanotube Transistors

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Nanoscale field-effect transistors (FETs) that employ an individual semiconducting carbon nanotube as the charge-carrier channel hold great potential for the realization of high-performance integrated circuits on glass or flexible polymeric substrates. There are two principal approaches to the design of integrated circuits based on field-effect transistors: In complementary circuits, both p-channel FETs and n-channel FETs are combined, while in unipolar circuits all FETs are of the same carrier type (i.e., either p-channel or n-channel FETs). In terms of static power consumption and noise integrity, complementary circuits are fundamentally superior to (and thus in principle preferred over) unipolar circuits. However, while there are many reports on p-channel carbon-nanotube FETs with excellent performance and stability [1-3], the realization of n-channel carbon-nanotube FETs with adequate performance and stability remains an unresolved challenge, so that integrated circuits based on carbon-nanotube FETs are often implemented in a unipolar topology with resistive load elements instead of n-channel FETs [1-3]. To realize unipolar carbon-nanotube circuits with good static and dynamic performance on glass or polymeric substrates we have developed a fabrication process in which transistors based on individual semiconducting carbon nanotubes are monolithically integrated with load resistors based on thin vacuum-evaporated and lithographically patterned carbon films. For the realization of the load resistors we have taken advantage of the fact that thin films of vacuum-evaporated carbon have a relatively large Ohmic resistance that matches well with the on-state and off-state resistances of the carbon-nanotube FETs.

To fabricate, characterize and integrate a large number of individual-carbon-nanotube transistors and thin-film carbon resistors, an array of metal probe pads and alignment markers was defined on the substrate. For each transistor a narrow gate electrode was then defined by electron-beam lithography and vacuum evaporation of 30 nm thick aluminum, connecting each gate electrode to one of the probe pads allocated for each transistor. The gate electrodes were then covered with a thin gate dielectric composed of oxygen-plasma-grown AlO_x (3.6 nm thick) and an octadecylphosphonic acid self-assembled monolayer (2.1 nm thick) [2,3]. The electron-beam resist was then removed by lift-off. Single-walled carbon nanotubes produced either by the high-pressure carbon monoxide (HiPCO) method or by the arc-discharge method and purchased from commercial sources were then randomly dispersed on the substrate from a liquid suspension that had been thoroughly sonicated and centrifuged prior to use. Using scanning electron microscopy (SEM), one individual carbon nanotube was then located on each of the patterned gate electrodes, its location and orientation was registered with respect to the alignment markers, and a pair of Ti/AuPd source and drain contacts was defined for each transistor by electron-beam lithography, metal evaporation, and lift-off. The transistors have a channel length of 300 to 400 nm.

To fabricate the load resistors, rectangular areas or meanders overlapping two adjacent probe pads were defined by electron-beam lithography, and a carbon film with a thickness of about 50 nm was deposited by vacuum evaporation and patterned by lift-off. Figure 1a shows a photograph of a glass substrate, an optical microscopy image of an array of transistors and load resistors fabricated on a glass substrate, and an SEM image of a carbon-nanotube transistor. Each substrate contains up to 35 nanotube transistors and up to 105 thin-film carbon resistors.

The current-voltage characteristics of all transistors and resistors in each array were then measured in ambient air at room temperature. The yield of functional nanotube transistors with an on/off current ratio of at least 10^4 (for V_{DS} = -0.1 V) is usually around 30% in the case of mixed (semiconducting and metallic) carbon nanotubes produced by the HiPCO method, 50% in the case of mixed nanotubes produced by the arc-discharge method, and about 80% in the case of sorted semiconducting nanotubes (IsoNanotubes-S, provided by NanoIntegris). Figure 1b shows the current-voltage characteristics of a transistor based on a semiconducting carbon nanotube produced by the arc-discharge method fabricated on a glass substrate. This transistor has an on/off current ratio of 10^7 for V_{DS} = -0.1 V and an on/off current ratio of 5×10^4 for V_{DS} = -1 V. The transconductance is 6 μS and the subthreshold swing is 80 mV/decade.

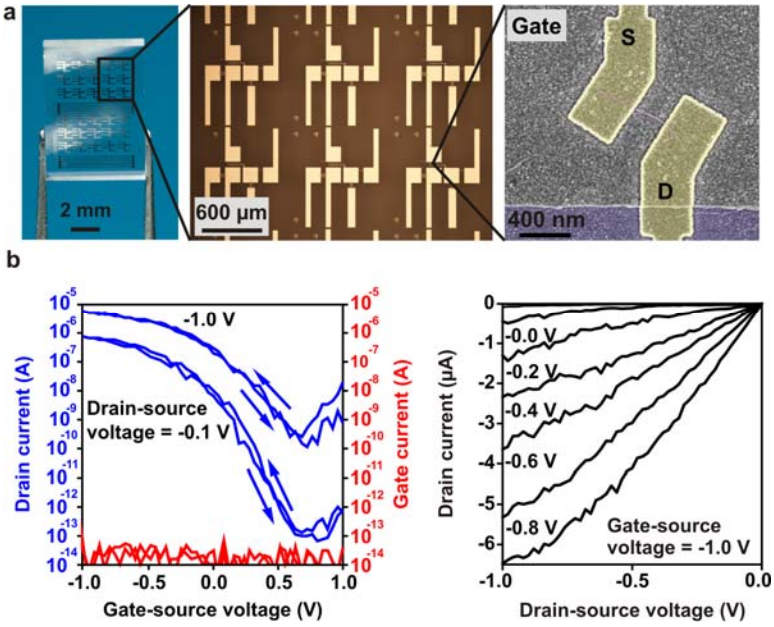

Figure 1:
(a) Photograph of a glass substrate, optical microscopy image of an array of carbon-nanotube transistors and thin-film carbon load resistors, and SEM image of a carbon-nanotube transistor. The local gate electrode, the source and drain contacts, and the gate/source and gate/drain overlap areas are clearly visible.
(b) Transfer and output characteristics of a transistor based on an individual semiconducting carbon nanotube produced by the arc-discharge method and fabricated on a glass substrate.

The simplest integrated circuit is the inverter which consists only of a field-effect transistor and a load resistor. Figure 2a shows the circuit schematic and a photograph of an inverter based on a carbon-nanotube transistor and a thin-film carbon load resistor with a resistance of 120 MΩ fabricated on a glass substrate. Because the load resistors are patterned directly between the probe pads for the output node (V_{OUT}) and the supply voltage (V_{DD}) node, there is no need for an additional process step to define interconnects. Figure 2b shows the static transfer characteristics and the small-signal gain of this inverter measured at a supply voltage of -1 V. As can be seen, the output signal swings completely from 0 V to V_{DD} (> 0.99 V) as the input voltage is changed between the on-state and the off-state of the transistor. The small-signal gain reaches about 15.

Owing to the fact that the load resistors are monolithically integrated with the transistors on a glass substrate, the parasitic capacitances are very small, and so the integrated inverters are able to switch large signals with relatively short delay. Figure 2c shows the dynamic response of an inverter to an input signal with a frequency of 2 MHz. When the input potential is changed from -1 V to +1 V, the transistor switches from the on-state to the off-state, and since the load resistance is smaller than the off-state resistance of the transistor, the output node is charged through the load resistor to the supply potential (-1 V). To minimize the time required for this transition, which is determined not only by the parasitic capacitances, but also by the load resistance, the load resistor of this inverter was designed to have a relatively small resistance (1.2 MΩ). The signal delay associated with charging the output node through the load resistor can be estimated by fitting an exponential function to the falling edge of the output signal of the inverter. In Fig. 2c this yields a signal delay of 100 nsec, which is significantly shorter than the signal delay of the carbon-nanotube circuits reported by Bachtold et al. [1], which were limited by the parasitic capacitances associated with the cables connecting the transistors to external load resistors. When the input potential is changed from +1 V to -1 V, the transistor switches from the off-state to the on-state, and since the on-state resistance of the transistor is smaller than the load resistance, the output node is discharged through the transistor to ground potential. The signal delay associated with this transition can be estimated by fitting an exponential function to the rising edge of the output signal of the inverter. In Fig. 2c this yields a signal delay of 12 nsec, which is the shortest signal delay reported for unipolar integrated circuits based on carbon-nanotube transistors.

The inverters shown in Fig. 2b and 2c require a positive input voltage (>0.2 V) to switch the transistor into the off-state, but the output voltage of the inverter is never positive, which means that the input and output voltages of these inverters do not match. As a result, this type of inverter cannot be cascaded, i.e. the output of this inverter cannot drive the input of an identical inverter. The reason for the positive switching voltage of these inverters is that our carbon-nanotube transistors often have a slightly positive threshold voltage (about +0.2 V for the transistor shown in Fig. 1b). Therefore we have designed and fabricated inverters with an integrated level-shift stage that consists of two thin-film carbon resistors (see Fig. 2d). The purpose of the level-shift stage is to shift the (negative) input signal by a few hundred millivolts towards a more positive potential required to switch the transistor into the off-state. As a result, inverters with integrated level-shift stage have matching input and output levels, i.e. inverters with level-shifting switch for input voltages between 0 V and -1 V and produce output voltages between 0 V and -1 V (see red curve in Fig. 2e).

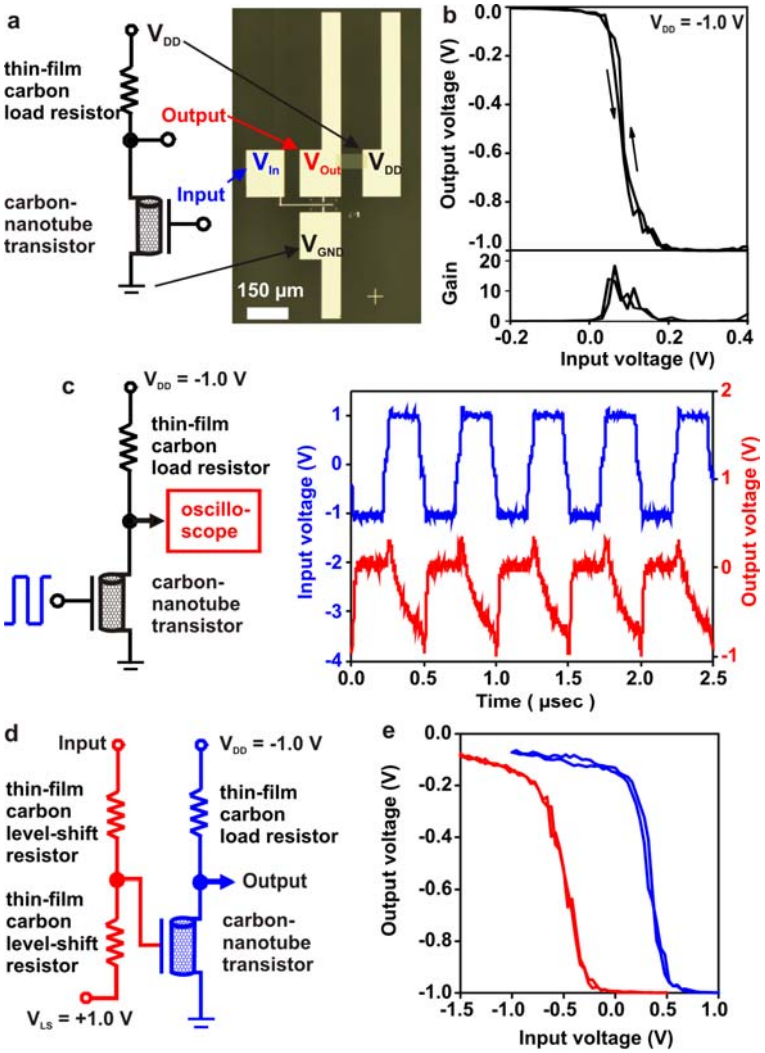

Figure 2:
(a) Schematic and optical microscopy image of an inverter composed of a carbon-nanotube transistor and a thin-film carbon load resistor.
(b) Static transfer characteristics of an inverter with a load resistance of 120 MΩ.
(c) Output response of a carbon-nanotube inverter to a square-wave input signal with a frequency of 2 MHz. The load resistance is 1.2 MΩ. By fitting an exponential function to the rising edge of the output signal, a time constant of 12 nsec is extracted for the switching delay of the transistor.
(d) Circuit schematic of an inverter with an integrated level-shift stage.
(e) Static transfer characteristics of inverters without (blue line) and with level-shift stage (red line).

Using our carbon-nanotube transistors and thin-film carbon resistors we have also realized a sequential circuit. In sequential circuits, the output signal depends not only on the present input (as in

combinational circuits), but also on the history of the input. Sequential circuits of transistors based on individual-carbon nanotubes have to our knowledge not been previously reported. Figure 3 shows the circuit schematic and the electrical response of an SR NAND latch (a type of flip-flop) based on carbon-nanotube transistors and thin-film carbon resistors. The circuit operates as follows: Applying a brief LOW pulse (pulse width 20 msec) to the S input causes the output (Q) to switch from the HIGH state (-1.5 V) to the LOW state (~0 V). This state information is stored in the latch, so that the output remains LOW until a LOW signal is applied to the R input which switches the latch (and the output) back to the HIGH state (see Fig. 3).

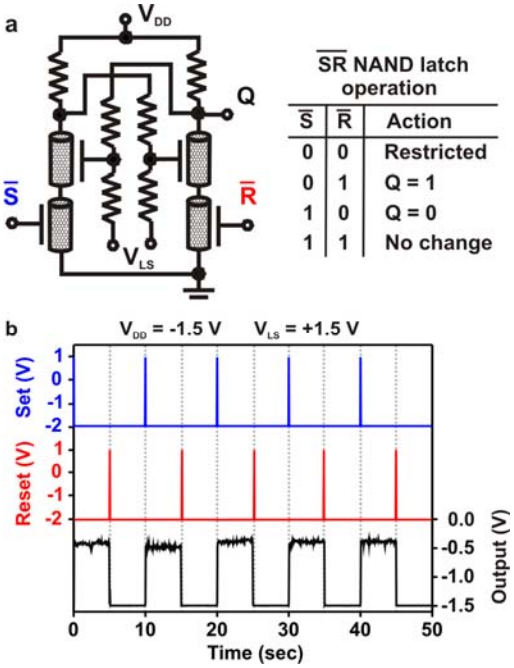

Figure 3:
Circuit schematic and input-output characteristics of an SR NAND latch realized using individual-carbon-nanotube transistors and thin-film carbon resistors.

In summary, we have fabricated unipolar integrated circuits using field-effect transistors based on individual carbon nanotubes with large transconductance (>1 μS), large on/off ratio (>10^4) and short switching delay time constants (12 nsec). Load resistors were realized using vacuum-evaporated and lithographically patterned carbon films that provide a resistance between 300 kΩ and 100 MΩ and good linearity of the current-voltage characteristics. To account for the slightly positive threshold voltage of the transistors, an integrated level-shift stage based on two additional thin-film carbon resistors was implemented. Fast integrated circuits like these are potentially useful for a variety of large-area electronics applications on arbitrary substrates, for example flexible information displays or conformable sensor arrays.

[1] *Bachtold, A., P. Hadley, T. Nakanishi, and C. Dekker.* Science **294**, 1317-1320 (2001).
[2] *Weitz, R. T., U. Zschieschang, A. Forment-Aliaga, D. Kälblein, M. Burghard, K. Kern, and H. Klauk.* Nano Lett. **9**, 1335-1340 (2009).
[3] *Ryu, H., D. Kälblein, O. G. Schmidt, and H. Klauk.* ACS Nano **5**, 7525-7231 (2011).